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Investigation of induced charge damage on self-aligned metal-gate MOS devices

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Investigation of Induced Charge Damage on Self-Aligned Metal-Gate MOS Devices

By

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ABSTRACT

MOS capacitors and NMOS transistors were fabricated with various gate oxides and inter-level dielectrics (ILDs) in order to study the effects of plasma induced charging during the post-metal plasma deposition of an insulating oxide layer. The gate oxides investigated include thermal SiO_2, a low temperature oxide (LTO) deposited by low pressure chemical vapor deposition (LPCVD) using silane and oxygen, and an oxide deposited by plasma enhanced chemical vapor deposition (PECVD) using tetra-ethyl-ortho-silicate (TEOS) as a precursor. A standard-recipe TEOS-based ILD was studied, as well as an alternative recipe that utilized decreased power. Additional wafers were fabricated with an LTO ILD to serve as a control group in order to isolate the influence of the ILD deposition on the respective gate dielectric. By studying C-V and I-V characteristics, both interfacial degradation as well as bulk charging was demonstrated as a result of the PECVD ILD deposition. The investigation demonstrated clear differences in plasma-induced charge effects on the various gate dielectrics. A correlation between the ILD deposition power and the resulting charge influence was established. In addition, post-plasma annealing experiments were done to study the thermal stability of induced charge.

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CHAPTER 1

INTRODUCTION

1.1 Process Damage in High Temperature CMOS

Since Jack Kilby's invention of the integrated circuit in 1958, the size of the field effect transistor has shrunk drastically in order to provide increasing computing power for modern day devices [1]. As transistor sizes continue to decrease, the gate oxide becomes increasingly more susceptible to process induced damage. When plasma is used in various fabrication steps, localized charge build up creates significant electric fields that produce tunneling current. Defects initiated by this tunneling current cause decreased breakdown voltages, increased interface states, increased leakage current, deteriorated oxide reliability and even decreased yield as oxides can break down during processing [2]. To meet scaling demands, gate oxides are now reaching thicknesses approaching 12-15Å [3]. As a result of this, the effects of plasma process induced damage are becoming an increasing concern. Figure 1.1 shows a typical modern day NMOS device that might face such process-induced degradation.

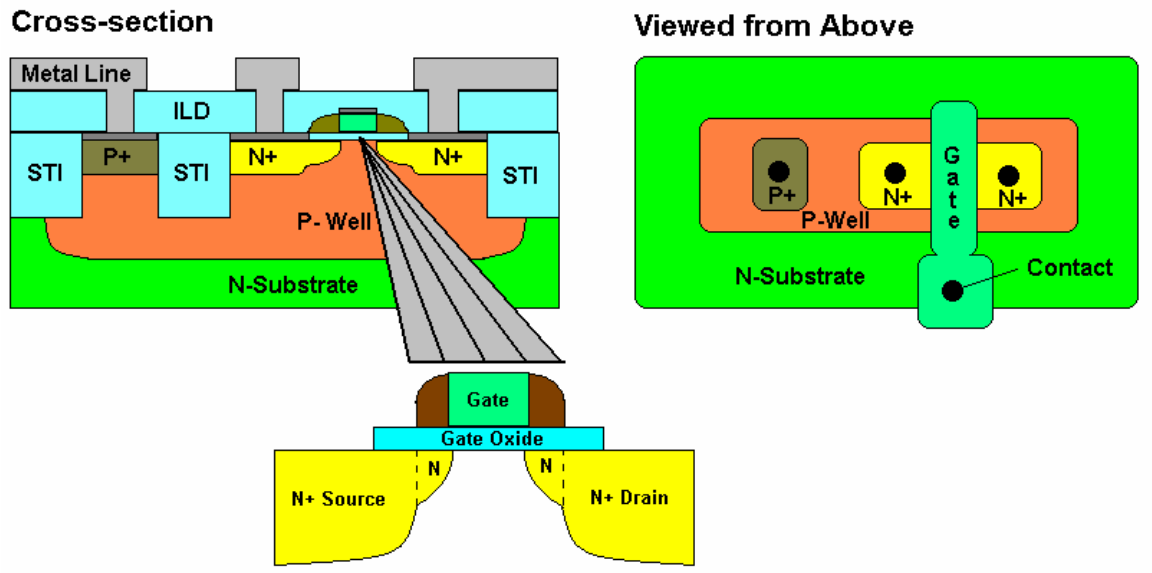

Figure 1.1: Cross-section of a modern NMOS transistor

Normal operation of the device would consist of grounding the source and applying a positive bias on the drain and gate. As the voltage on the gate increases, electrons from the boron-doped (p-type) well accumulate beneath the gate oxide to form an inversion channel. Subsequently current flows from the source to drain and the device is considered to be on. When an ultra-thin gate oxide is broken or severely degraded during plasma processing, current flows from the source directly through the oxide reaching the gate. When this happens the gate loses complete control over the source to drain current and the device is rendered useless.

The device shown in Figure 1.1 is fabricated on bulk silicon wafers, where thermal constraints are relatively relaxed. This means that the devices can be processed at higher temperatures (above 900°C) without causing structural damage to the substrate. In most cases, this can allow for a significant portion of process-induced damage to anneal. Fortunately, the majority of integrated circuit applications use devices fabricated on a bulk silicon substrate.

1.2 Process Damage in Low Temperature CMOS

Low temperature processes are specifically of interest in the area of Thin Film Transistor (TFT) research. TFTs are used in applications such as liquid crystal displays (LCDs) as a means of switching the pixels on and off. In order to transmit light for displays, they must be fabricated on a clear glass or plastic substrate. As a result, thermal constraints become more stringent in order to prevent the substrates from melting or deforming during processing. This generally limits useable process temperatures to below 600°C [4].

Since low temperature CMOS processes are done below 600°C, thermal oxides cannot be practically grown and used as gate dielectrics, as in standard technology. Low temperature oxides (LTO) or silicon nitrides are needed as gate dielectrics because of this. Dielectrics deposited at lower temperatures (compared to a thermal oxide) exhibit structural inferiority resulting in higher leakage currents and lower breakdown strengths. These effects are directly correlated with plasma induced charging. Furthermore, low temperature CMOS processes are limited in the ability to anneal out this damage, leaving devices even more vulnerable to process induced degradation. Figure 1.2 shows a typical TFT that would need to be processed at low temperatures.

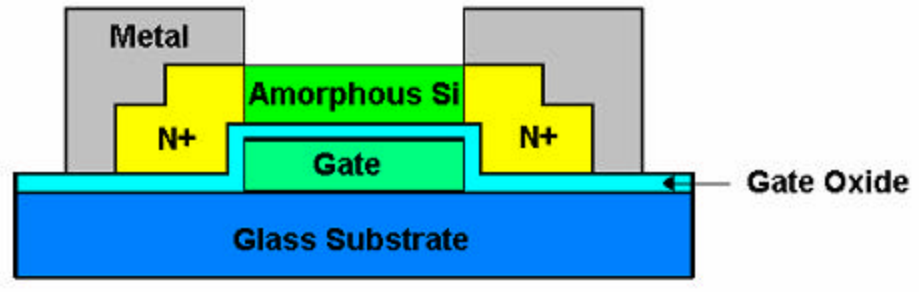

Figure 1.2: Typical bottom gate TFT processed at low temperatures

Despite being upside-down, the TFT shown above operates the same way as the transistor in Figure 1.1. TFTs usually have a similar bottom gate design. The dielectric and amorphous silicon are then deposited on top of the gate. This configuration saves a lithography step that would ordinarily be needed to pattern for the source/drain implants; the wafer is simply coated with resist and flood exposed through the transparent substrate resulting the self-aligned source/drain pattern.

1.3 Motivation

RIT has been developing a low temperature TFT process to characterize a new silicon-on-glass substrate material under development by Corning, Incorporated. Because processing temperatures must be low, as dictated by the glass strain point [5], and gate oxides are of inferior quality compared to a thermally-grown oxide, significant effects of induced charge damage have been observed [26]. This work focuses on characterizing such effects in deposited oxides using devices fabricated on bulk silicon wafers at both low and high process temperatures.

CHAPTER 2

LOW & HIGH TEMPERATURE DIELECTRICS

This chapter presents information on a variety of insulating materials that have been implemented in industrial applications in order to meet the requirements of low temperature processing constraints with acceptable dielectric performance.

2.1 Thermal Oxidation

Thermal oxidation is a well-known process that results in a durable, high quality film with minimal charge levels. Most importantly, the interface between silicon and thermally grown SiO_2 contains less dangling bonds and interface-trapped charge as compared to deposited dielectrics. For such applications, as thin film transistors that require process temperatures below 600°C, it is not practical to use an atmospheric-pressure thermally grown oxide as the gate dielectric. While high-pressure oxidation can be used to grow SiO2 to a practical thickness for this application, the film quality is compromised significantly [6].

2.2 Chemical Vapor Deposition (CVD)

There are three main techniques used for CVD of dielectric materials for semiconductor applications. This section describes the techniques, their applications, and associated advantages and disadvantages.

APCVD

Atmospheric Pressure Chemical Vapor Deposition (APCVD) is the simplest of the various CVD deposition techniques. A predetermined mixture of reactant and diluting inert gas is used to transport gas species in a reaction chamber to the substrate. In such a CVD system there are two types of reactions that occur. First, what is called a homogeneous reaction occurs in the reactor's atmosphere. When this occurs, aggregates of the material being deposited form in the gas phase and adhere to the surface of the substrate forming low-density films with many defects. The second type of reaction that occurs in the system is known as a heterogeneous reaction. In the heterogeneous reaction, gas reactants are adsorbed on the substrate (which is heated) where they react to form a high quality deposited film. This is, therefore, the favorable reaction in vapor deposition. In an APCVD deposition, the reactions are limited by the amount of gas reaching the surface, also known as being in the mass-transport-limited regime. After the reactions occur, remaining gaseous by-products are then desorbed from the surface and removed from the chamber [7].

LPCVD

Low Pressure Chemical Vapor Deposition (LPCVD) is very similar to APCVD. The main difference is the decreased pressure. LPCVD is typically done at 0.25-2.0 torr and temperatures between 550°C and 700°C. Because of the decreased pressure, films are deposited in the reaction-rate-limited regime. At low pressure, diffusivities of reactant gases are increased such that their transfer to the substrate doesn't limit growth rates. Because of this, the growth rate is ultimately controlled by the surface reaction,

which is dominated by temperature. Temperature control in LPCVD tools is very accurate. Therefore, film uniformities of LPCVD films are superior to those deposited by means of APCVD. Also, lower pressure decreases the unwanted homogeneous gas-phase reactions. This results in higher quality films that have less contamination than those deposited by APCVD [6].

PECVD

Plasma Enhanced Chemical Vapor Deposition (PECVD) is a deposition method that uses plasma to excite reactive gases in order to help dissociate them at lower temperatures. Two electrodes, one of which is the chuck holding the wafer, form the plasma under a vacuum with regulated gas flow. Free electrons are accelerated in the electric field causing both elastic and inelastic collisions with the gas molecules. The inelastic collisions result in dissociation and ionization of the gas molecules as well as secondary electrons. Dissociated gaseous ions utilize a heterogeneous reaction on the wafer surface to form the deposited film [8].

Each of these deposition techniques has different advantages, disadvantages and applications. Some of these can be seen in Table 2.1.

CVD Process	Advantages	Disadvantages	Applications
APCVD	Simple, Fast Deposition, Low Temperature	Poor Step Coverage, Contamination	Low-temperature Oxides
LPCVD	Excellent Purity, Excellent Uniformity, Good Step Coverage, Large Wafer Capacity	High Temperature, Slow Deposition	High-temperature Oxides, Silicon Nitride, Poly-Si, W, WSi_2
PECVD	Low Temperature, Good Step Coverage	Chemical and Particle Contamination	Low-temperature Insulators over Metals, Nitride Passivation

Table 2.1: Comparisons of APCVD, LPCVD and PECVD [7]

2.3 DIELECTRICS FOR LOW TEMPERATURE APPLICATIONS

This section describes physical and electricdal properties of various gate dielectrics that have been used in low temperature applications.

2.3 PECVD Silicon Nitride (SI_3N_4) as a Gate Dielectric

Traditionally, TFT's have been fabricated using amorphous silicon with a bottom gate design in order to maximize throughput. (Back-side exposure can result in self-aligned source and drains when fabricating bottom gate transistors on a transparent substrate saving a lithography step and mask level.) With the bottom gate design, a metal gate is deposited, followed by the Si_3N_4 dielectric and the amorphous silicon surface is deposited last. The Si_3N_4 gate dielectric promotes a good interface between the channel and dielectric when the amorphous silicon (a-Si) is deposited on top of it. It is done in this order specifically to optimize device characteristics influenced by surface morphology, density of states and charges at the interface between the dielectric and

channel. Device characteristics directly affected by the interface are effective mobility, on current, off current, and sub-threshold slope [9].

The nitride thin films can be characterized by both chemical as well as physical properties. Chemical properties such as the Si/N ratio or Si-H and N-H concentrations can affect etch rates, band gap and permittivity. Silicon rich nitride films exhibit better interface quality but higher permittivity and leakage. Nitrogen rich films show lower permittivity and leakage, but a less desirable interface with more stress. With excess nitrogen, density of interface states at mid-gap increases resulting in mobility degradation [9]. Increased nitrogen content has, however, been found to increase the band gap as high as 5eV and decrease deposition rates [10]. Elevated hydrogen content increases etch rate (good for tight critical dimension control), and passivates dangling bonds in the bulk as well as at the interface. On the downside, excess hydrogen results in Si-H bonds which lead to charge trapping when Si3N4 is used as the gate dielectric [9]. For this case, N-H bonds are preferred over Si-H. Using a low temperature (~180C) and SiH4/N2 gas flow, a very low hydrogen content in the form of Si-H can be achieved [10].

Physical properties such as surface roughness and stress also affect device performance. Roughness of the nitride surface contributes to dangling bonds and interface states, which decreases mobility. A rough surface can be the result of suboptimal deposition conditions such as too high of a power or a hydrogen concentration that is too high. Mismatched silicon content and band energy causes stress at the interface of the Si_3N_4 dielectric and silicon. This causes bonds to break forming interface states. Stress at this interface is significantly lower when a nitride dielectric (especially silicon rich) is chosen to be in direct contact with the silicon surface [9].

Si_3N_4 has thus far been the dielectric of choice because its interface characteristics with amorphous silicon. Its preferred method of deposition is PECVD over LPCVD because of throughput and the ability to coat uniformly over large areas for display applications. The reactants used can be seen in Equation 2.1 below. The main disadvantage of the nitride dielectric to this point is leakage current.

$$SiH_4(gas) + NH_3(or\_N_2)(gas) \xrightarrow{200-400^{\circ}C\_rf} Si_xN_yH_z(solid) + H_2(gas)\ [6] \qquad (2.1)$$

2.4 PECVD Oxide as a Gate Dielectric

PECVD oxide having reasonable integrity for a gate dielectric has been achieved at low temperatures by means of a few different strategies. Low temperature oxide films have been deposited with PECVD by combining silane with nitrogen/nitrous oxide, and by the use of TEOS (tetraethylorthosilicate) and oxygen with argon. The following equations show how $Si0_2$ is formed with these gas flow combinations [11-13]:

$$SiH_4(gas) + 2N_2O(gas) \rightarrow SiO_2(solid) + 2N_2(gas) + 2H_2(gas)\ [6] \qquad (2.2)$$

$$SiH_4(gas) + O_2(gas) \rightarrow SiO_2(solid) + 2H_2(gas)\ [6] \qquad (2.3)$$

$$Si(OC_2H_5)_4(liquid) + O_2(gas) \rightarrow SiO_2(solid) + by-products(gas)\ [6] \qquad (2.4)$$

Studies have shown that SiH_4 with N_2O and N_2 can deposit device quality SiO_2 gate dielectrics for TFT applications, by using a high-density inductively coupled plasma, controlling ion energies and achieving a high deposition rate. In doing so, the deposited

oxide will exhibit more desirable electrical characteristics more closely resembling thermal SiO_2. Specifically, bulk oxide traps (formed by H_2 gas by-products reacting to make Si-H and Si-OH charge trapping structures) are reduced by utilizing such deposition parameters [13].

For a deposited film formed by SiH_4 with N_2O and N_2, film density and refractive index are directly related to silane flow. Lower silane flow rates result in more porous films with lower densities, and higher silane flow rates result in denser films with higher refractive indices closer to those of thermal oxides [13]. Lower N_20 and N_2 gas flows also result in denser films. Near stoichiometric films are deposited with little or no nitrogen gas flow. [6]. FTIR has shown that SiO2 deposited with these gas flows for gate dielectrics have exhibited little or no Si-OH, O-H or Si-H bonds. These films also showed high physical breakdown fields (11.6MV/cm) [13], low leakage current (1.7e-8 A/cm^2 at 2MV/cm) and low interface trap densities ($2.6x10^{10}$ states/cm^2/eV). FTIR data also suggests that films deposited at a higher power have higher density. This may be due to higher lateral mobilities of gas species on the film surface. Mobility of impinging species results in structural rearrangements during deposition leading to denser films with fewer pores. Higher power also produces higher energy bombardment resulting in the removal of loosely bound fragments and weak bonds [13].

PECVD oxide has also been investigated for TFT applications using TEOS (tetraethylorthosilicate), as seen in equation 2.4 [12]. When attaining a stoichiometric film, it has been found that O_2 in O_2: TEOS ratios from 10:1 to 20:1 are needed to minimize traces of carbon and nitrogen in the oxide [6]. This incorporated oxygen is only effective at higher RF powers (>250W). With lower RF powers, O_2 is not dissociated

and incorporated into the film, resulting in a silicon rich film with a higher density [12]. Increased substrate/deposition temperatures have also been correlated to lower density SiO_2 films, which are oxygen rich. Both of these dependencies have been verified by FTIR and observed in etch rate changes. (Oxygen rich films etch more rapidly than silicon rich films) [12]. Unlike films deposited with silane and nitrogen/oxygen, Si-OH and O-H bonds appeared to be evident from FTIR peaks. These charge traps are a result of TEOS decomposition reactions and are responsible for high leakage currents ($2.8x10^{-5}$ A/cm^2 at 2MV/cm). TEOS based films have shown good field strength (E_{bd} of 10.6 MV/cm) suggesting good film quality, similar to that of silane and nitrogen/oxygen based films [12].

As with silicon nitride gate dielectric films, the interface quality is very important for providing good electrical characteristics. With PECVD oxide films, this is more of a problem than with nitride. Surface roughness and dangling bonds at the silicon interface cause interface trap states that dramatically affect device performance. To minimize these affects, different cleaning processes have been implemented. In-situ cleaning processes have been attempted with CF_4 +O_2 as well as O_2 plasmas prior to deposition [12].

The CF_4 +O_2 plasma treatment has been used in an attempt to provide a cleaner surface for the deposition. Unfortunately the CF_4 leaves organic polymers at the surface resulting in electrical charges at the Si/SiO_2 interface. For this reason it has been found to be impractical. The O_2 plasma treatment grows a thin layer of oxide at the interface before deposition. This was found to improve the actual interface, but resulted in an increased density of impurity damage at the interface, also making it less practical. As

far as these plasma treatments, a standard RCA clean has been determined to be more effective [12].

Similar attempts at plasma treatments have been made using helium. It has been found that a helium plasma treatment prior to a deposition consisting of diluted SiH_4/helium, N_2O and helium carrying gas. The silane dilution with helium resulted in a much slower deposition rate, ~14Å/s, and higher quality PECVD oxide; an E_{bd} of 9MV/cm^2, an interface trap density of $6x10^{10}cm^{-2}eV^{-1}$, and a fixed charge of $6x10^{11}cm^{-2}$ have been obtained [11].

2.5 Multiple Layer Gate Dielectric Stacks

Because single layers of PECVD oxide and nitride suffer from low breakdown strength, high interface trap density and high gate leakage current, combinations of the two can be used to optimize electrical characteristics. Two common PECVD gate stack approaches use an oxynitride/oxide and oxynitride/nitride/oxide (ONO) stacks.

Oxynitride, or SiON is grown as the interface layer using N_2O plasma for the oxynitride/oxide dielectric stack. Using oxynitride rather than oxide or nitride at the dielectric/silicon interface provides decreased surface roughness. Decreased interface roughness and strong Si-N bonds provide a reduction of interface traps compared to using PECVD oxide or PECVD nitride dielectrics alone. This results in a great increase in TFT field-effect mobility. AFM measurements showed a significant decrease in surface roughness when the oxynitride layer is employed at the silicon interface. Because the oxynitride layer is very thin and leaky, PECVD oxide is needed on top to provide strength and resistance to leakage current. High breakdown fields (8.5MV/cm), low

leakage current, and low interface trap density and good long-term reliability have been reported using this dielectric stack [14].

Similar to the oxynitride/oxide stack, the ONO gate dielectric stack uses an oxynitride layer, grown by N_2O plasma, at the silicon interface for the reasons stated above. It also employs a nitride layer in the middle. This layer helps further reduce leakage current, increases the breakdown field to 9.4MV/cm, and allows for a near equivalent capacitance with layers almost twice as thick (due to the higher permittivity of the nitride) [15].

2.3 CVD Dielectrics Investigated in this Study

This focus of this study is on the influence of plasma processes on SiO_2 gate dielectric materials deposited using LPCVD and PECVD techniques. The LPCVD film consisted of a Low-Temperature Oxide (LTO) deposited using silane (SiH_4) and oxygen reactants. The PECVD process used TEOS as the precursor, with oxygen added in the process recipe. Thermal SiO_2 was used as a control; an assumed best-case resistance to plasma-induced charge damage.

CHAPTER 3

ANALYSIS TECHNIQUES

3.1 Capacitance Measurements

Information from capacitance voltage (C-V) measurements can often provide a wealth of information relating to the dielectric, the semiconductor and the interface between the two. To measure a capacitance, an AC signal is applied to the device. From a ratio of the voltage input and measured current, an impedance value of the capacitor structure is calculated. A high gain operational amplifier then acts as a current-to-voltage converter. This output voltage is then compared to the input voltage by means of a phase detector. The circuit can be seen in Figure 3.1.

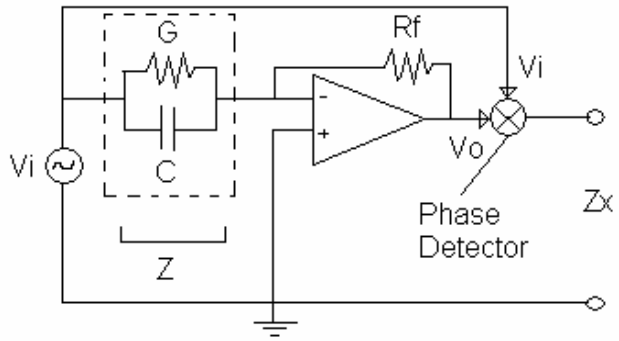

Figure 3.1: Circuit diagram of capacitance-conductance meter [16]

From the circuit configuration in Figure 3.1, impedance for the device can be represented using the following equations:

$$Z = -\frac{R_F v_i}{v_o} \quad [16] \tag{3.1}$$

$$Z = \frac{G}{G^2 + (wC)^2} - \frac{jwC}{G^2 + (wC)^2} \quad [16] \tag{3.2}$$

The first term of the second equation represents conductance while the second is the susceptance term. The 0º phase angle corresponds to the conductance and the 90º-phase angle corresponds to the susceptance (capacitance) value. [16]

3.2 C-V MEASUREMENTS

In order to obtain important information regarding a dielectric and substrate of a MOS structure, the previously described capacitance measurement is taken for a range of DC biases across the device. When doing so, three distinct behaviors of the MOS structure affect the capacitance measurement. These are accumulation, depletion and inversion, as seen in the following Figures for a p-type substrate. Figure 3.2 shows the distribution of charge in the P-type MOS structure and how it should correlate to an ideal C-V curve. In order to understand how accumulation, depletion and inversion are related to the C-V curve, it is helpful to qualitatively look at each separately.

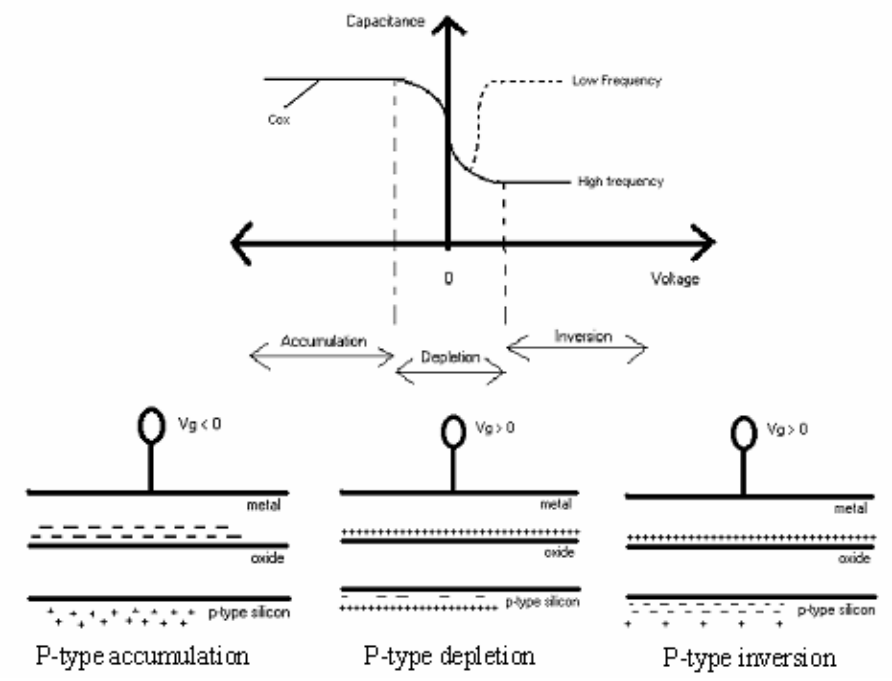

Figure 3.2: Accumulation, depletion and inversion as related to the C-V curve (p-type)

During accumulation, the DC bias causes majority carriers (holes for the p-type substrate) to pileup at the interface of the dielectric. For most semiconductor doping levels, majority carriers will respond quickly enough to slightly add or subtract charge from the two sides of the oxide at AC measurement frequencies up to 1 MHz. Since this relatively small amount of charge is added or subtracted close to the edges of the insulator, the charge configuration basically equivalent to an ordinary parallel-plate capacitor. Whether a low or high probing frequency is used, the capacitance is equal to the oxide capacitance as seen in Equation 3.3:

$$C_{acc} = C_{ox} = \frac{e_o \, k_{ox} A}{x_{ox}} \quad [16] \tag{3.3}$$

Where e_o is the permittivity of free space, k_{ox} is the dielectric constant, A is the area of the capacitor, and x_{ox} is the thickness of the dielectric.

Under depletion, a DC bias repels majority carriers from the oxide/silicon interface. This results in an effective width from the interface being depleted of majority carriers. The depletion width, W, fluctuates with AC bias as well as varies directly with the DC bias. Because the depletion width is dependent on bias, the capacitance of the semiconductor changes as seen in equation 3.4:

$$C_s = \frac{k_s e_o A}{W} \quad [16] \tag{3.4}$$

As a result of the fact that the semiconductor capacitance is in series with the oxide capacitance, the effective capacitance during depletion is that of Equation 3.5.

$$C_{depl} = \frac{C_{ox} C_s}{C_{ox} + C_s} = \frac{C_{ox}}{1 + \frac{k_o W}{k_s x_{ox}}} \quad [16] \tag{3.5}$$

where C_s is the semiconductor capacitance, W is the width of the depletion layer and k_s is the dielectric constant of the semiconductor.

The behavior associated with depletion comes to an end upon inversion. At this point, minority carriers begin to pileup at the oxide/semiconductor interface in response to the DC bias. Unlike accumulation and depletion, inversion is affected by AC probe frequency. Inversion C-V characteristics, therefore, act differently for low and high AC probe frequencies.

For a low probe frequency, minority carriers have enough time to be generated or annihilated along with the AC signal. This essentially results in the AC states behaving like a succession of DC states where charge is being added or subtracted close to the edges of the dielectric. For this situation, the capacitance approaches $C_{ox,}$ just as it did in accumulation.

For a high probe frequency, minority carriers are unable to be supplied or eliminated in response to the AC signal. The number of minority carriers at the inversion layer then becomes fixed and the depletion width just fluctuates about a maximized depletion width $W_{dm.}$ This width is represented by Equation 3.6.

$$W_{dm} = \sqrt{\frac{4e_{si}kT\ln(N_a / n_i)}{q^2 N_a}} \quad [17] \tag{3.6}$$

With W forming a maximum of $W_{dm,}$ and an inadequate time for generation of minority carriers, the inversion capacitance for a high frequency measurement is as follows:

$$C_{inv} = \frac{C_{ox}Cs}{C_{ox} + C_s} = \frac{C_{ox}}{1 + \frac{k_{ox}W_{dm}}{k_s x_{ox}}} \quad [17] \tag{3.7}$$

Accumulation, depletion and inversion of an N-type semiconductor is qualitatively the same, except the majority carrier is the electron, and the C-V curve is mirrored about the C-axis [18].

3.3 Interface Trap Density Distributions

There are many methods to extract interface trap density by using C-V measurements. One of the most accurate techniques is referred to as the Kuhn method. To extract Dit by this method, the semiconductor capacitance C_s is correlated to the low frequency capacitance C_{lf} with the following equation:

$$D_{it} = \frac{1}{q}\left(\frac{C_{OX}C_{LF}}{C_{OX} - C_{LF}} - C_S\right) \text{ [16]} \tag{3.8}$$

The semiconductor capacitance is C_S is determined by Equation 3.9:

(3.9)

$$C_{S,LF} = \hat{U}_S \frac{K_s e_o}{2L_D} \frac{e^{U_F}(1-e^{-U_S}) + e^{-U_F}(e^{U_S} - 1)}{\sqrt{\exp(U_F)[\exp(-U_S) + U_S - 1] + \exp(-U_F)[\exp(U_S) - U_S - 1]}}$$

Where: $U_S = normalized\_surface\_potential = \frac{qf_S}{kT}$

$$U_F = normalized\_Fermi\_potential = \frac{qf_F}{kT}$$

$$L_D = \text{int}rinsic\_Debye\_length = \sqrt{\frac{K_S e_o kT}{2q^2 n_i}}$$

$$\hat{U}_S = sign\_of\_surface\_potential = \frac{|U_S|}{U_S}$$

As seen in equation 3.9, Cs is dependent on surface potential, but C_{LF} is a function of gate bias. In order to solve for the interface trap density, as seen in equation 3.8, a relationship must correlate surface potential to gate bias. This relationship is as follows:

$$f_S = \int_{V_{G1}}^{V_{G2}} (1 - \frac{C_{LF}}{C_{OX}}) dV_G + \Delta \quad [16] \qquad (3.10)$$

where ? is an integration constant given by the surface potential at $V_G = V_{G1}$.

Choosing V_{G1} and V_{G2} such that the integration is carried out from accumulation to strong inversion solves the integral above. The Kuhn method fits experimental and theoretical C_{LF} versus surface potential. The lateral voltage shift between the experimental and theoretical curves is equal to the integration constant relating surface potential to gate voltage. With C_{LF}, C_S, and the integration constant correlating VG to F_S, Dit can be determined over the entire band gap using equation 3.8. A typical interface trap density distribution can be seen below in Figure 3.3 [16].

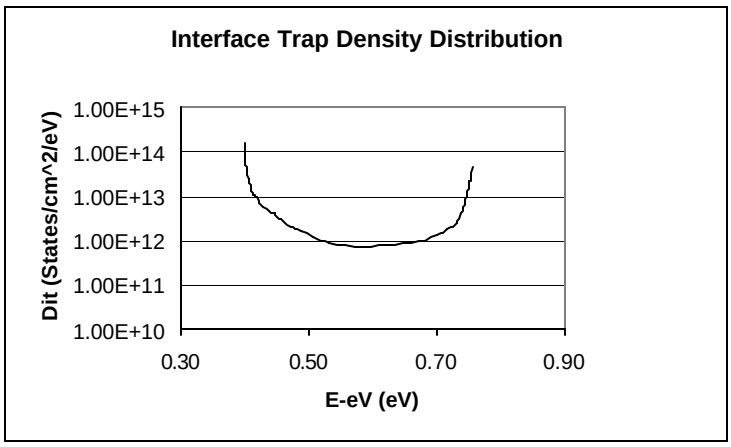

Figure 3.3: D_{IT} for TEOS SiO_2 capacitor using the Kuhn method

3.4 Breakdown and Leakage Measurements

Current-Voltage measurements can be used to determine breakdown fields and leakage currents of oxides. The oxide in a MOS capacitor physically breaks down when a high enough voltage is applied across it. To measure the breakdown field, Voltage is plotted against current as shown in Figure 3.4.

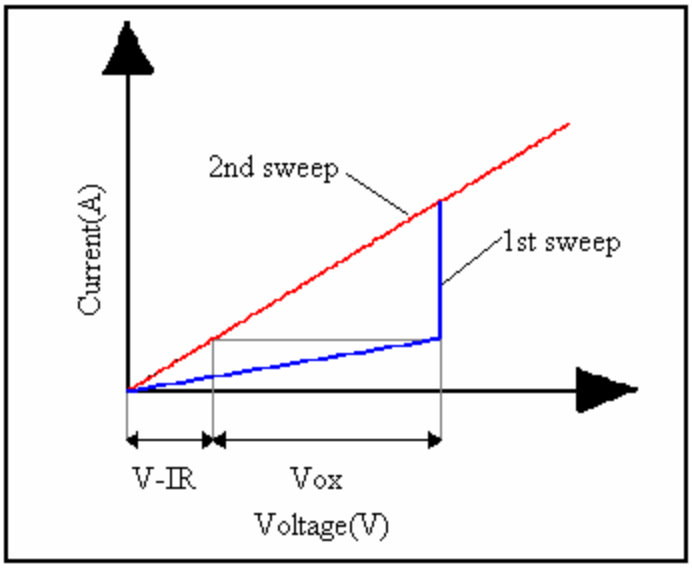

Figure 3.4: I-V breakdown measurement

The capacitor is wired in series with a 1MO resistor and swept twice. The first sweep physically breaks down the oxide, while the second sweep provides an I-V curve corresponding (very closely) to the resistor in series. The current measured at the point of breakdown is matched with a current on the second sweep. The voltage at which these currents meet corresponds to the potential drop across the wafer. From this the voltage drop across the oxide is deduced. To determine the breakdown field, the voltage drop across the oxide is divided by the oxide thickness. By using this method, leakage currents can be taken at any given field up until the point of physical breakdown.

3.5 Mobile Charge Measurements

There are two C-V tests that can be used to measure mobile ion content in a dielectric film. The first is a temperature bias stress test. After an initial C-V curve is taken, the wafer is heated to an elevated temperature (250°C-300°C) and a voltage stress is induced for a short period of time (~5-10 min.). When a negative stress is applied, positive mobile ions move to the surface of the dielectric in contact with the metal effectively increasing V_{fb} and shifting the C-V curve to the right. When a positive stress is applied, mobile ions move down to the silicon interface decreasing V_{fb} and shifting the C-V curve to the left. After the wafer is stressed at a high temperature, it is cooled down and the C-V measurement is taken. This is done twice, once with a positive stress and once with a negative stress. The voltage shift between the two C-V curves (that were oppositely stressed) corresponds to the mobile ionic charge according to the following equation: [6]

$$N_M(/cm^2) = \frac{\Delta V(e_o e_{ox})}{q(t_{ox})} \quad [6] \tag{3.11}$$

The second method of measuring mobile charge in a dielectric film is the triangular voltage sweep (TVS) method. For this experiment, a negative stress is applied at a high temperature to attract all of the mobile ions to the top of the dielectric. A high temperature, low frequency C-V curve is then done sweeping from positive to negative voltages. Mobile ions then travel from the top of the dielectric film down to the interface with the silicon as the bias changes from positive to negative. This ion current results in a peak in the measured capacitance. The area under the peak is then related to the mobile ion content by equation 3.12.

$$N_M = \frac{\int I(V)dV}{RqA} \quad [16] \tag{3.12}$$

In Equation 3.12, the integral in the numerator is equal to the area under the capacitance peak, R is equal to the sweep rate (V/s), q is the charge of an electron and A is the area of the capacitor (cm^2).

The TVS measurement is also able to determine if there are more than one mobile ionic species within a dielectric. When this is the case, there will be two separate capacitance peaks. This occurs when there is a difference in mass. Atoms with a lower diffusivities move slower, so they form broader peaks that are on the left. Ions with higher diffusivities move faster and form a narrower capacitance peak.

3.6 Current-Voltage for Transistor Parameters

A transistor has two modes of operation, linear and saturation. Their biasing conditions are shown for an n-channel MOSFET in the following relationships below.

$V_g > V_t$
$V_D < (V_G - V_t)$ Linear operation [19]

$V_g > V_t$
$V_D > (V_G - V_t)$ Saturation operation [19]

In the linear regime, the inversion layer extends all the way from the source to the drain. The drain current is also a function of the drain voltage such that higher drain biases result in increased drain current. In saturation mode, the drain bias is high enough to pinch off the inversion channel near the drain. Electrons in the channel region are pulled through the pinched off region at the saturation drift velocity as a result of the high longitudinal electric field. This allows for the drain current to be maximized and no longer a strong function of drain bias [19]. When testing transistors, they are typically tested using I-V curves in both linear and saturation regimes.

CHAPTER 4

PLASMA-INDUCED CHARGE DAMAGE

4.1 Introduction

Plasma is needed in MOSFET processing for many fabrication steps such as sputtering, etching, photoresist ashing, and dielectric deposition. In certain cases, it allows for decreased processing temperatures. Exposure to plasma may result in damage from unwanted chemical reactions, electron-hole pair creation, and oxide charging. Of these, the most significant source of damage to the modern sub-quarter micron transistor is gate oxide charging [20]. The gate oxide has a specific vulnerability to such processing steps because it is fragile and must tolerate high applied electric fields, both during processing and in device operation.

When exposed directly to plasma, a high electric field can be dropped across the gate oxide. Gate oxide degradation occurs when the field across it is high enough to produce Fowler-Nordheim (F-N) tunneling current from the bulk silicon to the gate [20]. This mechanism is responsible for breaking bonds at the silicon/SiO_2 interface, as well as resulting in an increased bulk oxide charge [20, 21]. It generally results in decreased lifetime and reliability of devices [20]. In some cases the field is high enough to result in a physical breakdown of the oxide, causing reduced yield.

Figure 4.1 shows band diagrams for the MOS structure at equilibrium (Vg=0) and at high field conditions. In part (A) the only way for an electron to get from the silicon to the gate metal is to directly tunnel through the entire energy barrier of the oxide, which is referred to as band-to-band tunneling. The probably of this happening is very low,

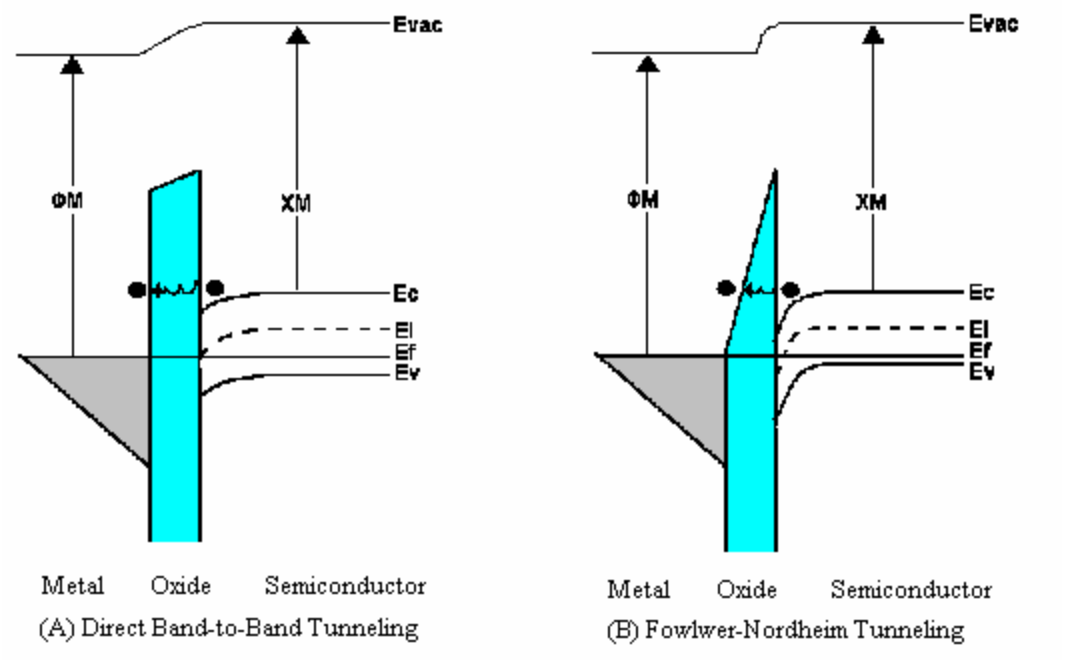

Figure 4.1: Direct band-to-band tunneling & Fowler-Nordheim tunneling [18]

especially for thicker oxides. Part (B) of Figure 4.1 shows the same band structure of the MOS device under a high electric field; a situation where the gate metal has a positive bias. With a high electric field the energy bands bend more abruptly, decreasing the thickness of the tunneling barrier and increasing the probability of a carrier tunneling. Tunneling under these conditions is referred to as F-N tunneling. This mechanism of current flow is responsible for the damage induced by high-field processing, as in most plasma processes. It is also worth noting that under typical bias conditions inversion may occur for p-type (boron-doped) silicon, allowing minority electron carriers to tunnel into the gate oxide. This can be seen in Figure 4.1 (B) where the Fermi level (E_F) is crossed by the intrinsic energy level (E_i), resulting in charge inversion at the surface.

The degree of gate oxide degradation is directly related to the field-induced F-N tunneling current, which is determined by factors such as the gate size and the size of

conducting surfaces connected to the gate. Metals connecting to the gate act as antennae structures that collect charge during plasma processing. The ability of these structures to collect charge is directly related to the gate oxide E-field experienced, and the resulting degree of damage to the dielectric layer. This quantity of charge is usually referred to as the antenna ratio. The antenna ratio is defined as the ratio of the area of conducting material over the thick oxide (that is connected to the gate) to the area of the gate. As this quantity increases, the extent of the damage done to the gate oxide will increase accordingly [20].

4.2 Electron and Hole Trap Generation

Charge trap centers in the bulk of an oxide are considered to be amphoteric meaning that they can become both negatively and positively charged. Trapped charge residing in the bulk of the gate oxide originates from weak Si-Si bonds where there is an oxygen vacancy between them; each silicon atom is back-bonded with three oxygen atoms (see Figure 4.2). The most common and widely accepted model to represent both electron and hole trapping is known as the HDL model (Harry Diamond Laboratories) [22, 23]. The HDL model suggests that the Si-Si bond is broken by free holes produced by radiation. This radiation could be from sources such as x-ray lithography [23], or plasma photo-generation [24]. The breaking of weak Si-Si bonds results in the formation of positive charge centers (filled hole-traps). These positive charge centers can remain charged, or combine with electron(s) and change their charge state [22]. A diagram of the HDL model for hole-trapping and electron-trapping is shown in Figure 4.2.

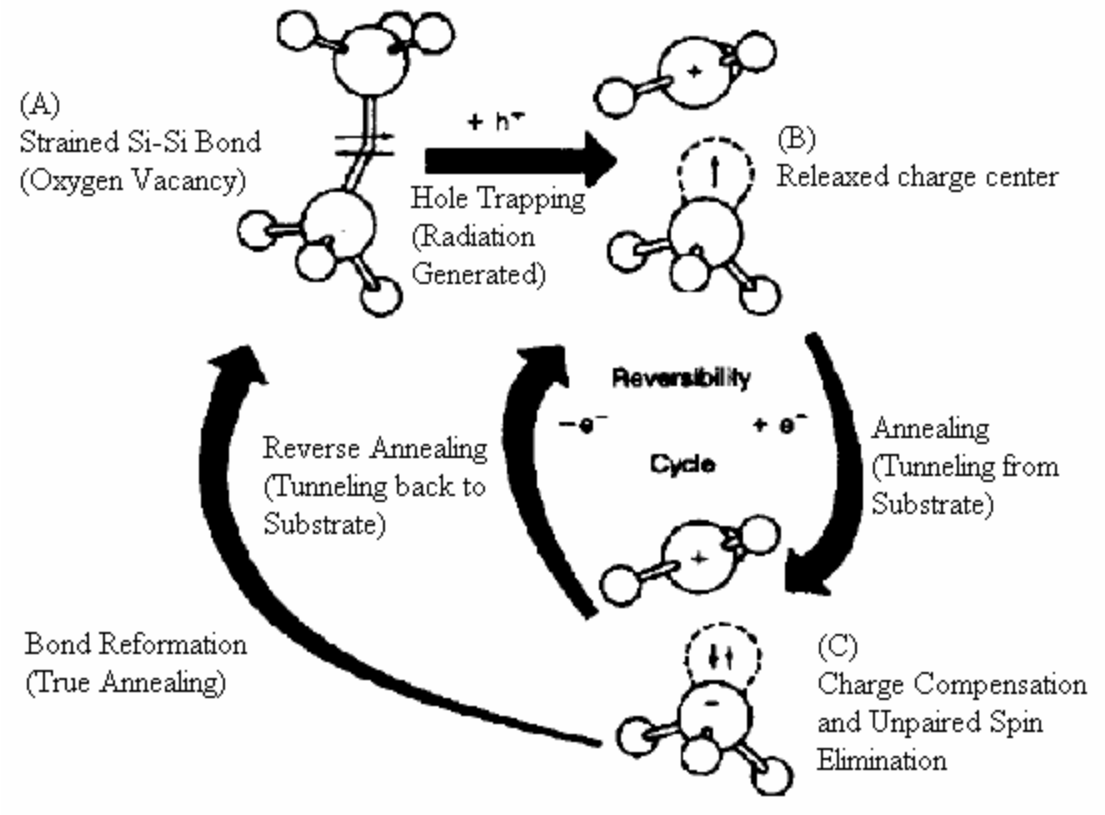

Figure 4.2: HDP model for hole & electron trapping [22]

Part (A) of Figure 4.2 shows the precursor of the charge trap before it is broken by the radiation-induced hole. As the hole breaks the Si-Si bond, it becomes trapped to one of the silicon atoms and moves away from the uncharged silicon atom. The hole-trap then takes on a relaxed configuration where the oxygen atoms become planar. At this point the trapped hole can be forward annealed by the application of a positive field across the oxide resulting in electrons from the substrate neutralizing the charge. A neutral dipole results upon capture of one electron [22]. From here, it can be reverse annealed, by applying a negative field across the oxide forcing the electron back toward the bulk. This returns the charge center back to the trapped hole seen in part (B) of the figure. If this doesn't happen, the neutral dipole acts as an electron trap and traps a second electron to become negative. From here it is possible for the charge center to recombine with the

neutral silicon atom by what is referred to as true annealing. A similar representation of this phenomenon can be seen in Figure 4.3.

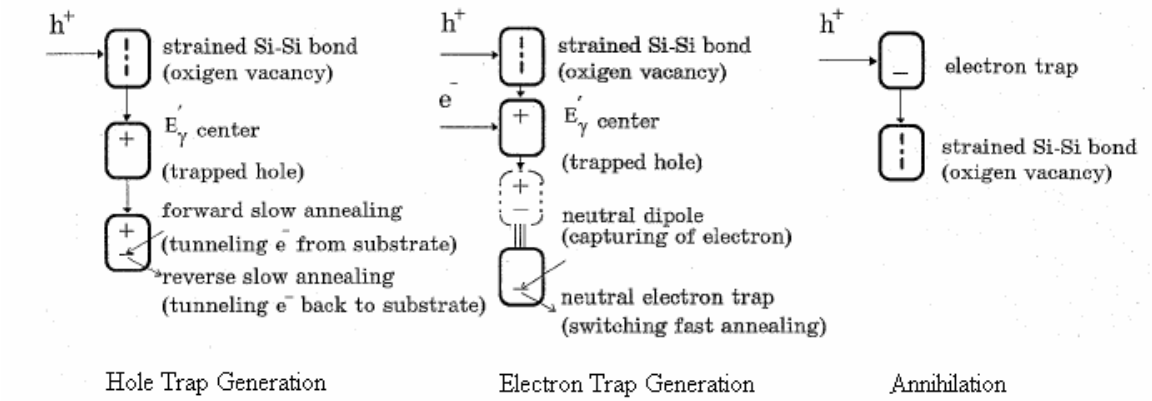

Figure 4.3: Electron and hole trap generation and annihilation processes [22]

4.3 Oxide Traps and Gate Leakage

Under rigorous operating conditions, elevated temperature and high-field conditions can cause the gate oxide integrity to degrade over time until it experiences catastrophic failure, known as breakdown. Common methods of determining resistance to failure are electric field breakdown (E_{bd}) tests, gate leakage measurements (below the E-field at which F-N or direct tunneling becomes significant) and charge to breakdown measurements (Q_{bd}). A desirable dielectric will have a high breakdown field, low gate leakage current and a high charge to breakdown value, which correspond to long device lifetimes.

Broken bonds and structural rearrangement associated with oxide traps can lead to higher leakage currents, as well as lower E_{bd} and Q_{bd} measurements. This has been confirmed by observing an increase in low-level leakage current subsequent to exposure

of a high field. The increase in leakage current is attributed to tunneling via stress-generated positive charge centers, local decreases in the tunneling barrier at defect sites, and trap assisted tunneling. The number of oxide traps generated by a high E-field has been shown to be proportional to the increase in leakage current [25].

When oxide traps are located in the bulk of an oxide, there are extra energy levels between the valence and conduction bands of SiO_2. With no trap states, an electron must obtain ~3eV in order to surmount the energy barrier between silicon and SiO_2 and contribute to current flow; the hole energy barrier is ~ 4eV [18]. Oxide traps present available energy states within the energy barrier that can act as stepping-stones for carriers to reach the conduction band. This makes it easier for charge to penetrate the oxide and assists in providing increased leakage current [18]. Note that a poor quality oxide layer may allow conduction through defect states without carriers surmounting or tunneling through the energy barrier.

4.4 Assessment of Plasma Induced Charge Damage

Both fully processed transistors and MOS capacitors can be used to assess plasma damage to thin oxides. Capacitors are preferred because of their short process time and ability to utilize wet processing for control samples in order to isolate the influence of particular plasma processes. Capacitance-Voltage (C-V) characteristics can be specifically used to determine interface trap densities by means of quasi-static measurements and the observed stretching in high frequency characteristics due to interface states. This allows a direct correlation between the creation of interface traps to specific plasma process steps. Unfortunately a representation of the entire process flow is

hard to capture using only capacitors. C-V data also may not provide adequate information regarding oxide charge trapping, as practical limitations on antenna ratios will not be consistent with values for actual transistors. For a more complete assessment of actual damage, it is usually necessary to fabricate transistors [20].

If transistors are fabricated, direct measurements of threshold voltage, gate leakage, sub-threshold swing, and transconductance can be made to characterize the influence of plasma damage. Bulk oxide trapping will result in increased threshold voltages and gate leakage while interfacial damage results in increased sub-threshold swings and decreased transconductance. Disadvantages of fully processed transistors to assess plasma damage include inability to accurately pinpoint critical process steps as well and difficulty in producing a reference with no plasma exposure [20].

For devices fabrication in this study, there are many process opportunities for the introduction of plasma induced damage. To isolate the influence of specific plasma processes and to avoid factor confounding, alternatives to plasma processes were used in certain situations (e.g. solvent photoresist strip instead of oxygen plasma ash). Processes where plasma induced damage are of primary concern include the metal gate sputter deposition, the gate reactive-ion etch (RIE), the inter-level dielectric deposition (ILD), and the contact/interconnect aluminum sputter deposition. The next chapter will describe the transistor fabrication process and the designed experiments used in this investigation.

CHAPTER 5

EXPERIMENTAL DESIGN & DEVICE FABRICATION

5.1 Capacitor Experimental Design

An LPCVD oxide is the current gate dielectric for low temperature CMOS processing at RIT. It was initially chosen over a PECVD oxide because it showed lower and more uniform interface trap densities. For large-scale manufacturing, a PECVD oxide is far more practical as it results in a more uniform film and much faster deposition rates. For this work, PECVD and LPCVD oxide films were both chosen for a study on the effects of remaining process-induced damage, following low and high temperature annealing. An anneal temperature of 600°C was implemented for the low-temperature process constraint, as this temperature represents an upper limit of most thin-film transistor (TFT) fabrication on glass substrate material. Annealing at higher temperatures (up to 900°C) was also investigated to determine the thermal stability of the oxide damage. Capacitors were fabricated using these annealing conditions to compare the dielectric characteristics of the oxide films.

5.2 Capacitor Fabrication

All wafers were given a standard RCA Clean to remove contaminants and native oxides and provide a pristine surface for film deposition. Table 5.1 shows the initial experimental design for a comparison of the three SiO_2 layers.

SiO_2 Material	Anneal Temp (N_2 Ambient, 2hr)
LPCVD LTO	600°C
LPCVD LTO	900°C
PECVD TEOS	600°C
PECVD TEOS	900°C
Thermal SiO_2	None

Table 5.1: Capacitor treatment combinations

Aluminum was evaporated, followed by capacitor gate patterning using a GCA g-line 5X reduction stepper. The aluminum was etched using Transene type-A aluminum etchant, followed by a solvent photoresist removal. Wafers were finally sintered in H_2/N_2 at 450°C for 30 minutes. Cross-sections of the process are shown in Figure 5.1.

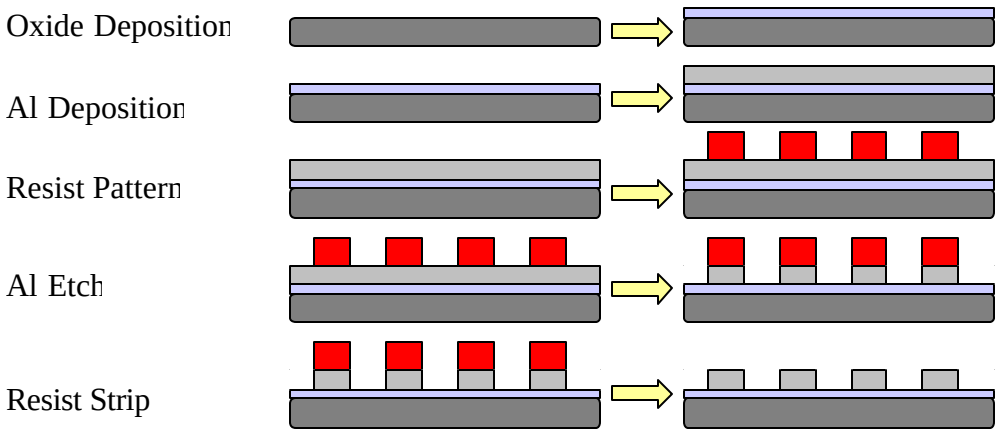

Figure 5.1: Cross-section of capacitor fabrication

5.3 Transistor Experimental Design

An experiment was designed to investigate the effect of plasma charging from the ILD deposition on metal-gate NMOS transistors. The standard low-temperature NMOS process utilized a 500? LTO gate oxide with a self-aligned molybdenum gate [26]. The devices were fabricated using the same oxide films as the capacitors identified in Table 5.1. Both the standard PECVD TEOS ILD recipe and a low power recipe were investigated. It was initially expected that when reducing the power for the ILD deposition, plasma damage would be less pronounced. This was based on the assumption that a lower power consisted of decreased voltage (not just current) resulting in a decreased field drop across the gate oxide during processing. Previous data suggests that the treatment combination with an LTO gate oxide and TEOS ILD annealed at 600°C exhibits significant charge damage [26]. Different annealing temperatures were implemented to determine the annealing conditions required to remove the damage. Table 5.2 shows the design space for the experiment. An LTO ILD was used as a reference (control) to isolate any observed differences to the PECVD TEOS ILD deposition (see last three treatment combinations in Table 5.2).

The screen oxide shown in Table 5.2 was a 500? film to protect the molybdenum gate during thermal processes and serve as a screen oxide for the source/drain implants. The standard PECVD oxide process was used for this thin screen oxide (with the exception of the last three treatment combinations) because process results indicated superior protection compared to the LTO film [26]. The PECVD screen oxide deposition time was extremely short (approx. 4sec); while this may induce some amount of damage

to the gate oxide, the process was consistent over the treatment combinations explored. Each treatment combination was done on a separate wafer.

Gate oxide	Screen oxide	ILD	Anneal Temperature (degrees C)
LTO	TEOS	TEOS	600
LTO	TEOS	TEOS	700
LTO	TEOS	TEOS	800
LTO	TEOS	TEOS	900
LTO	TEOS	LP TEOS	600
LTO	TEOS	LP TEOS	900
Thermal	TEOS	TEOS	600
Thermal	TEOS	TEOS	900
Thermal	TEOS	LP TEOS	600
Thermal	TEOS	LP TEOS	900
TEOS	TEOS	TEOS	600
TEOS	TEOS	TEOS	900
TEOS	TEOS	LP TEOS	600
TEOS	TEOS	LP TEOS	900
TEOS	LTO	LTO	600
LTO	LTO	LTO	600
Thermal	LTO	LTO	600

Table 5.2: Designed-experiment treatment Combinations

5.4 Transistor Fabrication

Transistors were fabricated using a CMOS process and mask set developed by Robert Manley and Robert Saxer [26]. Slight changes were made to simplify processes and only make NMOS transistors. Four-inch lightly doped p-type (100) wafers were used.

Step 1: RCA clean

A standard RCA clean [27] was first done in order to remove any initial contamination prior to processing. The clean process is shown in Table 5.2 shows the makeup of different chemical baths used. The APM bath is used to remove organic contamination while the HPM bath helps remove metallic contamination. HF is used in the process to remove any native oxide that may be on the silicon surface. Wafers were then dried in a spin-rinse-dry (SRD) machine.

Step 2: Well Implant

The well implant was done using the B_{11} species of boron at an energy of 170KeV and a dose of $1.2x10^{13}$ ions/cm^2. This dose was high enough to eliminate the need for a channel stop implant.

Step 3: Well Drive

A 500? pad oxide was grown and the well implant was driven in at 1000°C for 25 hours in nitrogen ambient. This was done to diffuse and activate well dopant into the silicon lattice. A cross-section of the device at this point is shown in Figure 5.2.

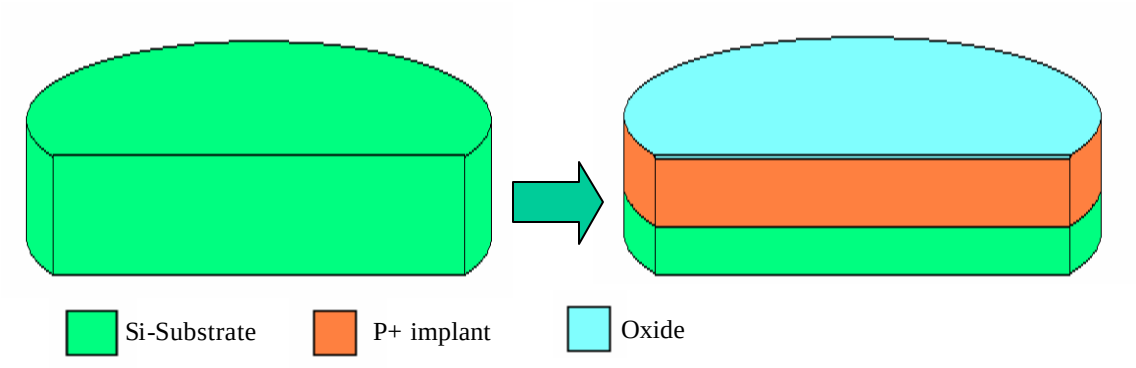

Figure 5.2: Cross-section of P-well and pad oxide formation

Step 4: Backside Implant

The backs of the wafers were implanted with B_{11} at an energy of 35KeV and a dose of $2x10^{15}$ ions/cm^2. This was done to provide a more ohmic back contact in order for the bulk silicon to be adequately grounded during testing.

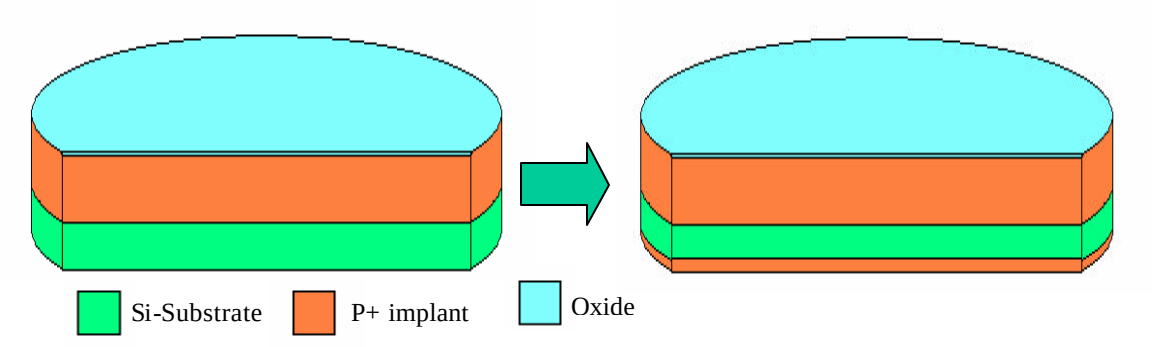

Figure 5.3: Back side contact implant

Step 5: LPCVD Field Oxide Deposition

A 4000? field oxide was deposited using LPCVD in order to create isolation between devices. A SiH_4 flow of 50sccm and an O_2 flow of 120sccm were used for a deposition time of 28.5 minutes. A cross-section of this step is shown in Figure 5.4.

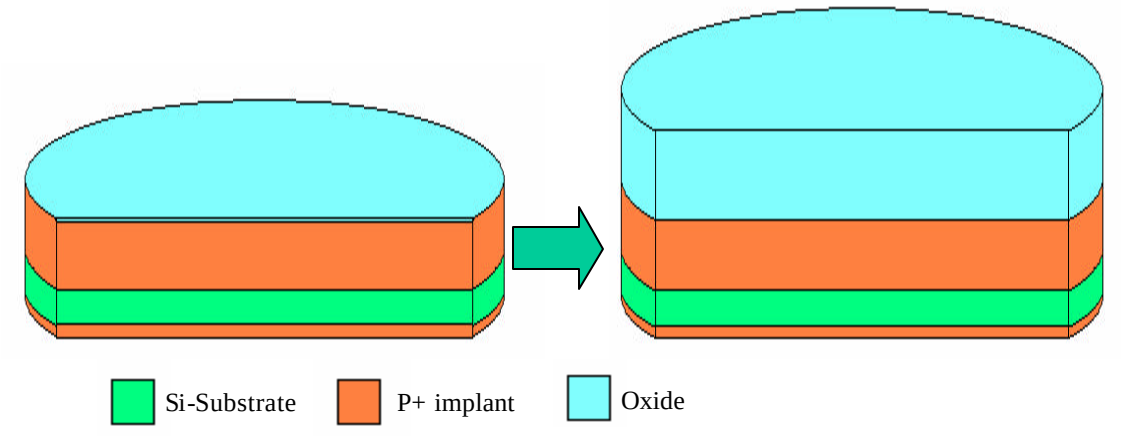

Figure 5.4: Field oxide deposition

Step 6: Backside Anneal

A high temperature anneal was done at 900°C in nitrogen for 10 minutes in order to activate the dopant from the backside implant. The anneal was also used to densify the field oxide.

Step 7: Active Lithography

Resist was patterned on top of the field oxide to define the active region. Rohm and Haas 1813 Resist was coated using an SVG wafer track on program 1. (See Appendix for details)

The wafers were exposed on a GCA g-line stepper for 0.64s using the EAGLEPLG program with pass 3. This pass exposes every die on the wafer except for 4. These were left to make embedded capacitors on each wafer. On this lithography step, pass 1 was used through a clear mask in order to open up the areas in the field oxide where capacitors were to be made. The wafers where then developed using recipe number 1 on the SVG track. (See Appendix for process details)

Figure 5.5 shows the cross-section of the devices after resist was coated, exposed and developed. The opening in the left of the Figure defines the active region for a transistor while the opening on the left defines the active region for a capacitor.

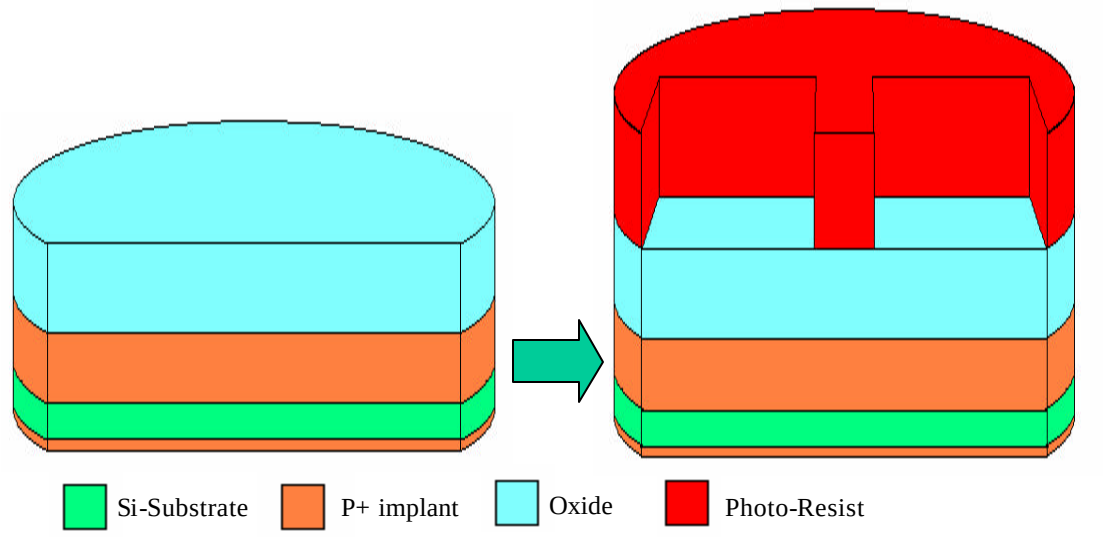

Figure 5.5: Active lithography

Step 8: Active Etch

The active etch was done in Buffered Oxide Etch (BOE) made up of 10 parts ammonium fluoride and 1 part HF. Wafers were etched in the BOE for 10 minutes, which corresponded to a 20% over-etch.

Step 9: Resist Strip

Resist was stripped using solvent strip at 70°C for 20 minutes. Wet resist removal was used for the entire experiment to rule out plasma charging from the photo-resist asher. After the resist strip, it was rinsed in DI water for 5 minutes and put through a spin-rinse-dry. The cross-section in Figure 5.6 shows the wafer processed up to this point.

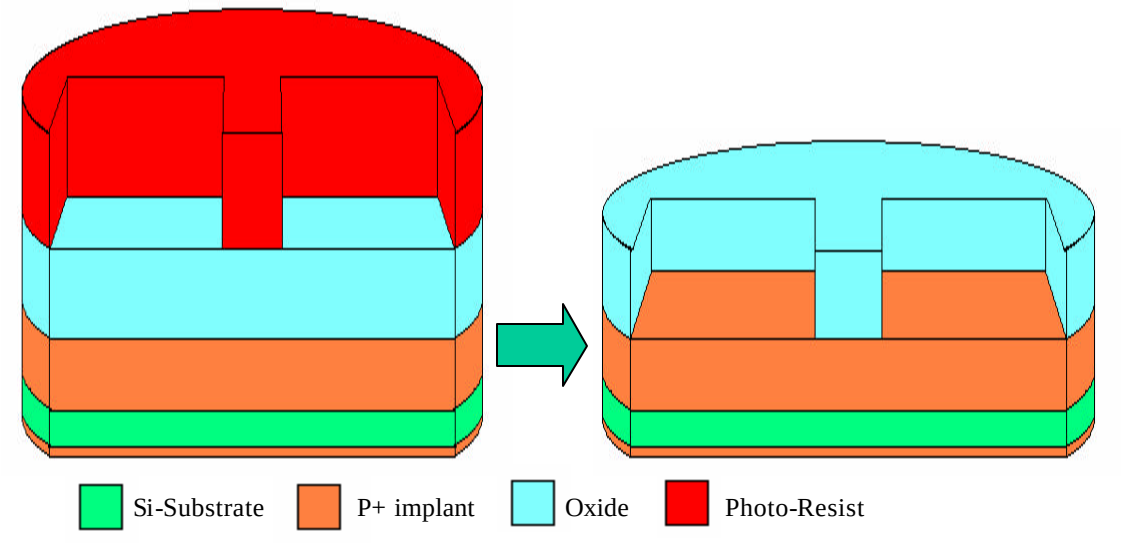

Figure 5.6: Active etch and resist strip

Step 10: Scribe wafers

Wafers were scribed in order to identify each treatment combination. They were purposefully scribed at this point rather than the beginning of the process. This was to ensure that defects from the scribe did not propagate through the wafer during the 25 hour anneal.

Step 11: RCA clean

The same RCA clean described in step 1 was used to ensure that the surface was pristine for the gate dielectric deposition.

Step 12: Gate Oxide Deposition

A target thickness of 500? of LPCVD oxide was deposited at 425°C with a SiH_4 gas flow of 50sccm and an O_2 gas flow of 120sccm. The deposition time was 2.73 minutes.

For the PECVD oxide, the PECVD TEOS deposition was conducted using an Applied Materials P5000. For 500? of PECVD oxide, conditions were a TEOS flow of 400sccm, an O_2 flow of 285sccm, a pressure of 9Torr, power of 205W, and a gap spacing of 220 mils. The deposition time was 4.4 seconds.

For 500? of thermal oxide, a BRUCE furnace was used. The oxidation temperature was 100°C and the O_2 gas flow was 10 lpm. The oxidation time was 42.5 minutes. Figure 5.7 shows the transistor cross-sections corresponding to the deposition of the gate oxide.

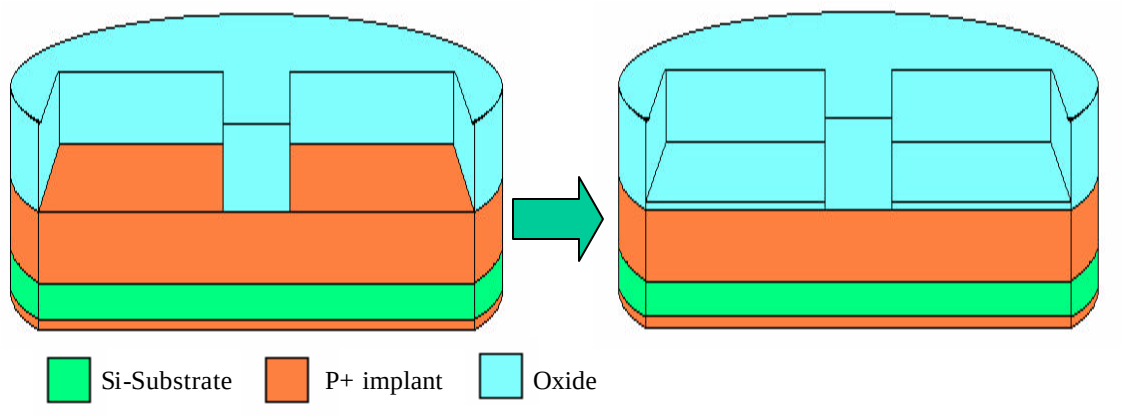

Figure 5.7: Gate oxide deposition

Step 13: Molybdenum Gate Deposition

Because of its high melting point, molybdenum was used rather than aluminum for the self aligned gate structure. It was sputtered with an RF sputtering tool with 15sccm of Ar. Base pressure was 7.5e-7Torr, deposition pressure was 14mTorr, forward power was 1000W, and reflected power was 0W. For the 5000? thick gate, the deposition time was 53 minutes. The cross-section is shown in Figure 5.8.

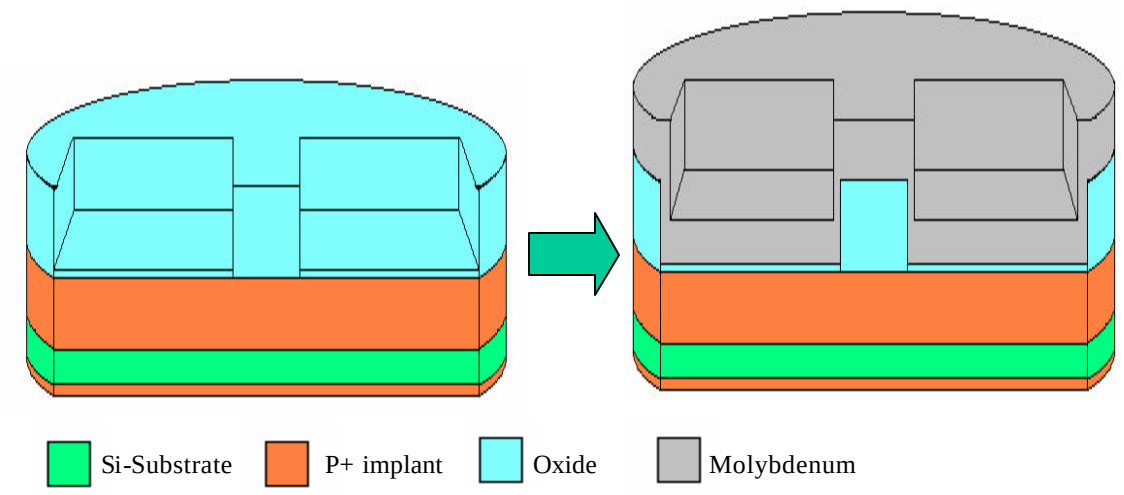

Figure 5.8: Molybdenum gate deposition

Step 14: Gate Lithography

Resist was coated with recipe 1 and developed with recipe 1 on an SVG wafer track as described in step 7. The EAGLEPLG program was used with pass 3 and the exposure time was 0.7s. This resulted in only exposing transistor die. The cross-section of this is shown in Figure 5.9.

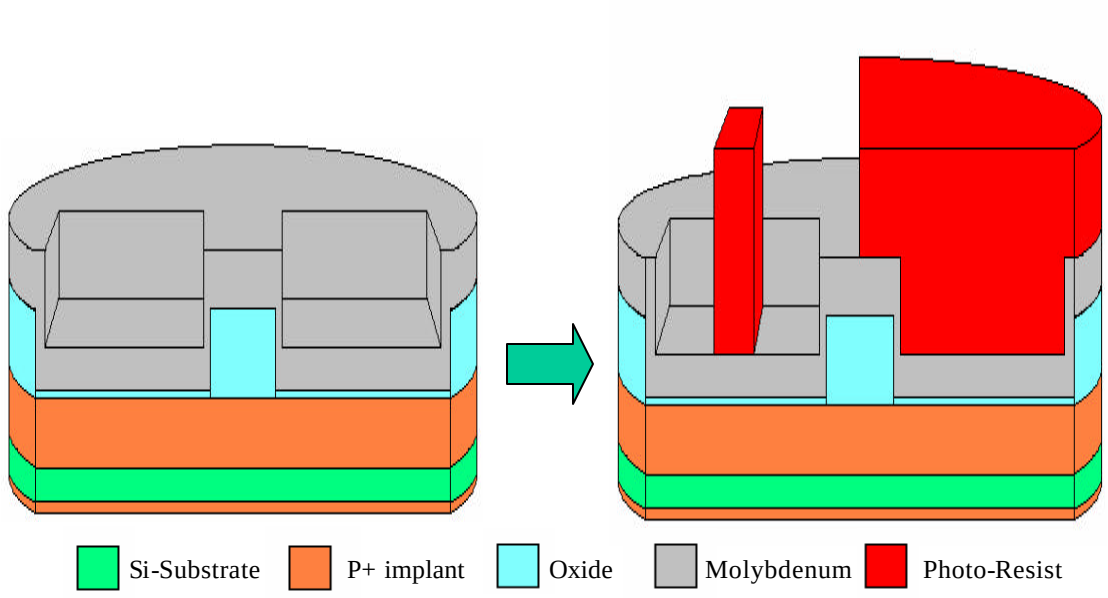

Figure 5.9: Gate lithography

Step 15: Gate Etch

The gate etch was done in a Drytec Quad reactive ion etcher. It was done with a power of 250W, a pressure of 150mTorr, and an SF_6 gas flow of 50sccm. The etch time was approximately 1.8 minutes.

Step 16: Resist Strip

Resist was stripped off using solvent strip as described in step 9. The cross-section of the device up to this point is shown in Figure 5.10.

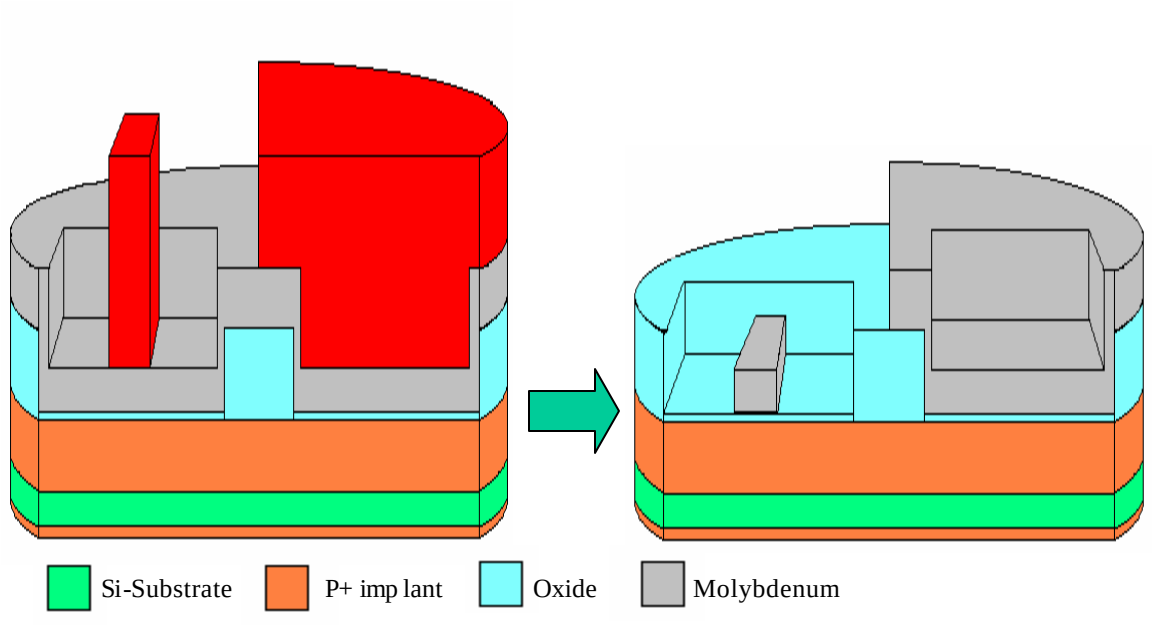

Figure 5.10: Cross-section after gate etch and resist strip.

Step 17: Screen oxide deposition

A 500? oxide was deposited over the molybdenum gate to protect it from oxidizing. It also served as the screen oxide for the source/drain implants. It was deposited with a power of 205W, a TEOS flow of 400sccm, an O_2 flow of 285sccm, a pressure of 9Torr,

and a gap spacing of 220mils. Control wafers received an LPCVD screen oxide deposited just as the gate oxide was. The cross-sections are shown in Figure 5.11.

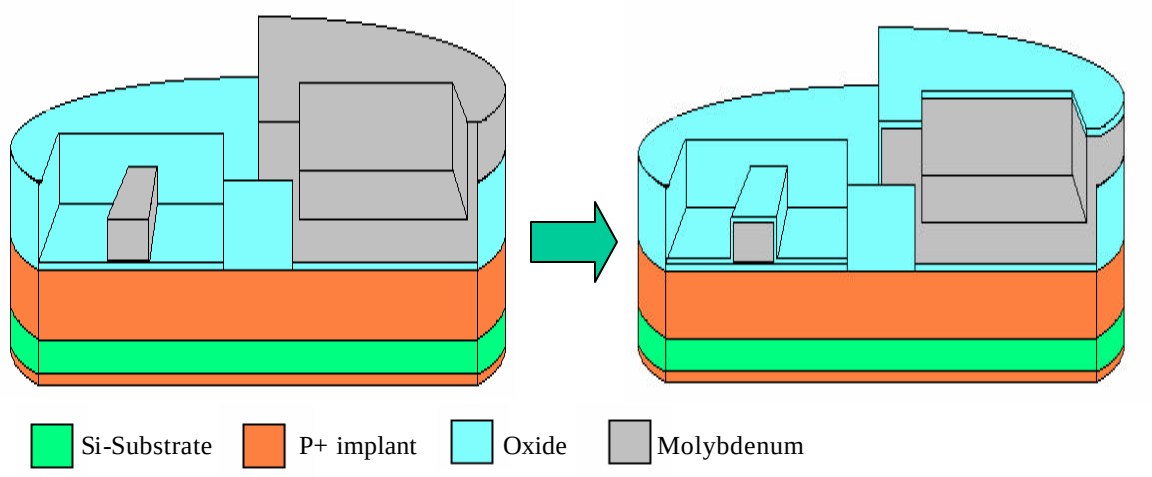

Figure 5.11: Cross-section of screen oxide deposition

Step 18: Source/Drain Implant

Source drain implants were done using a Varion 350D ion implanter. P_{31} species of phosphorous was implanted with a dose $4x10^{15}$ ions/cm^2, and an energy of 110KeV. A cross-section of the device after the source/drain implant is shown in Figure 5.12.

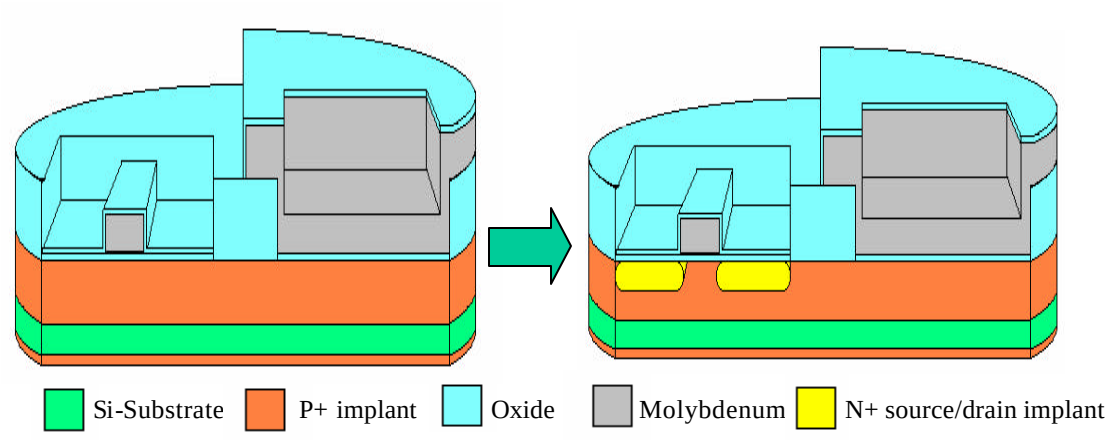

Figure 5.12: Cross-section of source drain implants

Step 19: Inter-Level Dielectric Deposition

For half of the experimental wafers, the standard TEOS ILD was deposited. This used the same parameters described in step 17. The deposition time was increased to 29.8s to obtain a thickness of 4000?. The other half of the wafers received a TEOS ILD deposited at a significantly lower power. A power of 50W was used instead of the standard 205W. Pressure was also decreased to 2.5Torr, TEOS flow was reduced to 100sccm, O_2 flow was reduced to 71sccm, and the gap spacing was adjusted to 215mils. The adjustments for this recipe were originally made by Germain Fenger to minimize stress in the ILD film. The three control wafers received an LPCVD deposition with the same gas flows and temperature as described in step 12. Deposition time was increased to 28.3 minutes to obtain a 4000? oxide. A cross-section of the ILD deposition is shown in Figure 5.13.

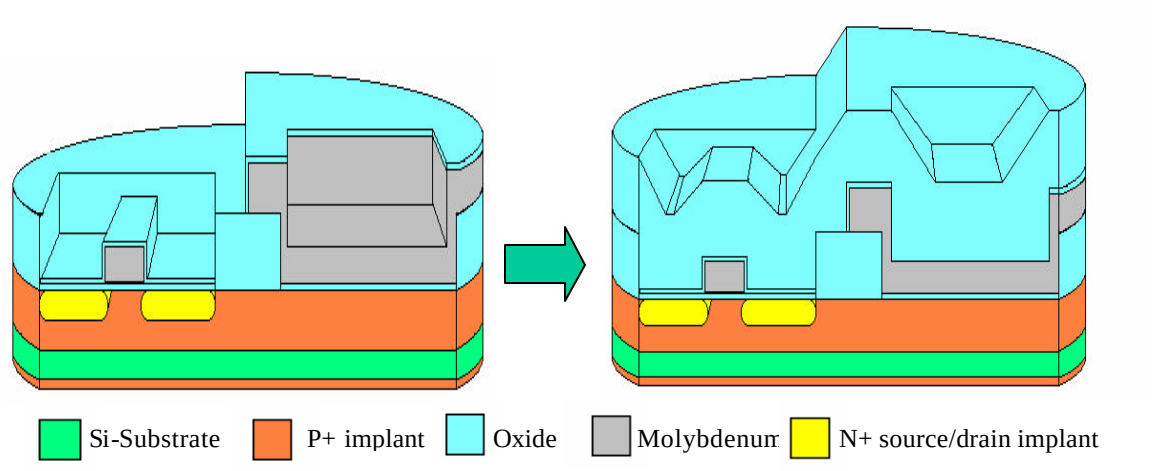

Figure 5.13: ILD deposition

Step 20: Contact Lithography

Contact lithography was done with the EAGLEPLG program with pass 3 to expose transistor die. Pass 1 was also used with a clear mask in order to remove the ILD for the capacitor die. Coat and develop recipes were the same as in step 7. The cross-section showing contact lithography is shown in Figure 5.14.

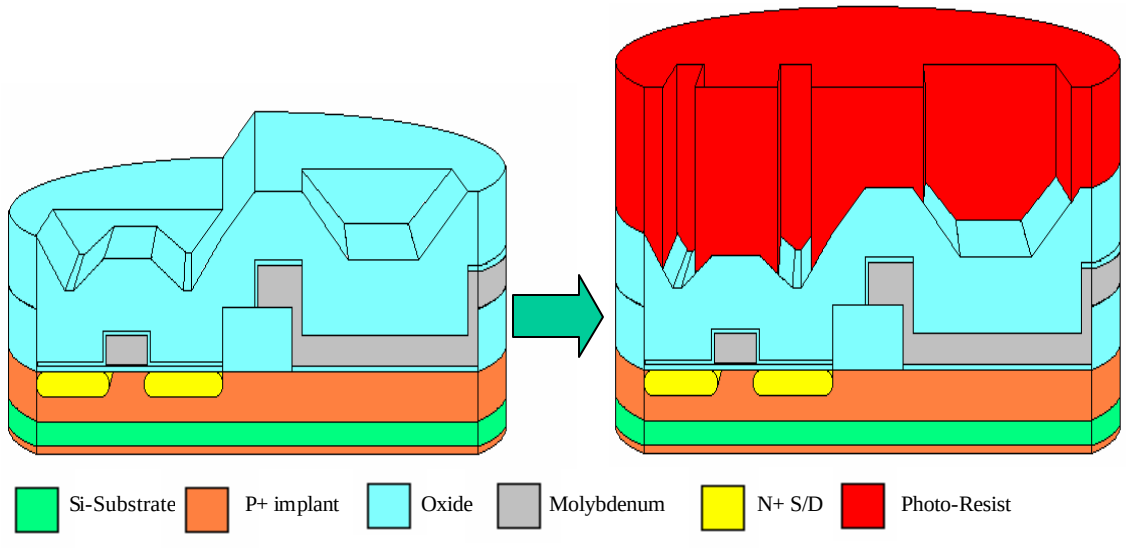

Figure 5.14: Contact lithography

Step 21: Contact Etch

The contact etch was done in Buffered Oxide Etch (BOE) made up of 10 parts ammonium fluoride and 1 part HF. 105% over-etch was used to ensure that the silicon was reached in order to provide an adequate contact for testing. This came out to be between 7 and 8 minutes for each wafer.

Step 22: Resist Strip

Resist was stripped off using solvent strip as described in step 9. The cross-section of device up to this point is shown in Figure 5.15.

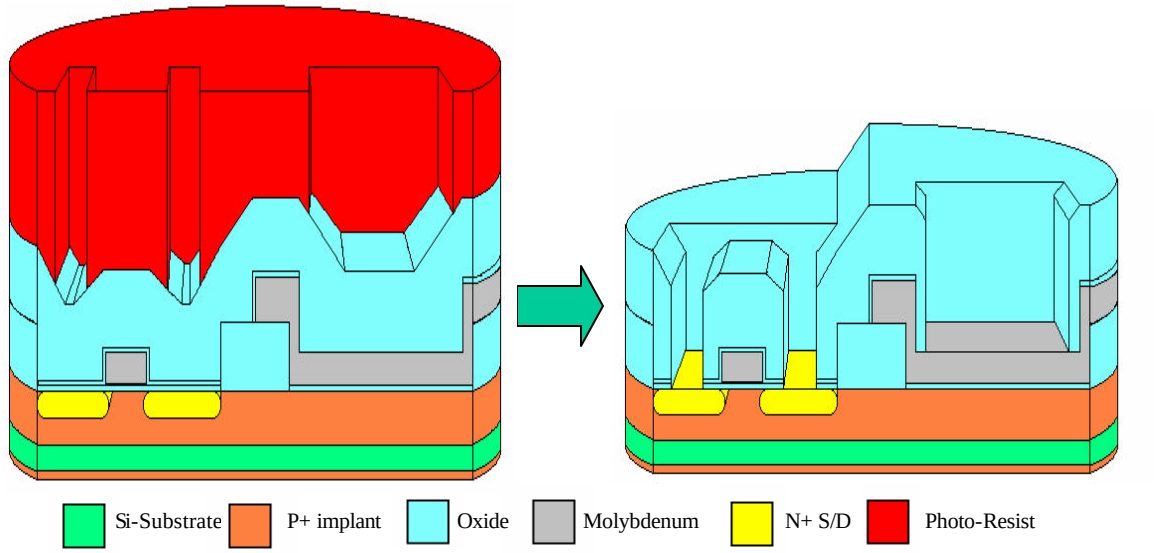

Figure 5.15: Contact etch and resist strip

Step 23: Aluminum Deposition

5000Å of Aluminum was sputtered using a CVC 601 DC sputtering tool. A power of 2000W, an Argon flow of 20sccm, and a pressure of 5mTorr were used for a deposition time of 18 minutes. This served as the metal to provide contact to the silicon, gate, substrate and capacitor areas. The cross-section illustrating this is shown in Figure 5.16.

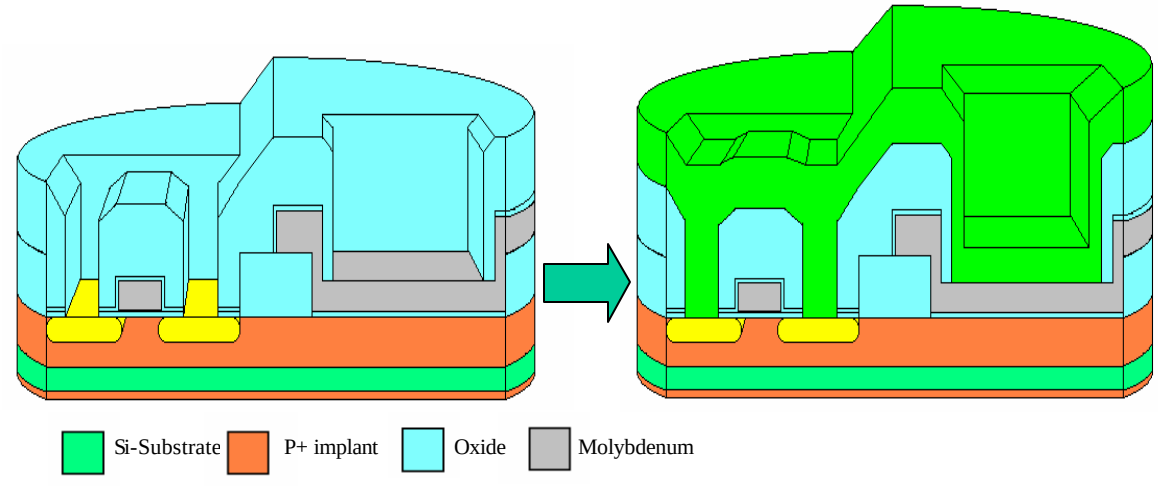

Figure 5.16: Aluminum deposition

Step 24: Aluminum Lithography

The aluminum was patterned in order to contact the transistors for testing. Resist was coated and developed as described in step 7 using the EAGLEPLG program on pass 3 to expose transistor die. Figure 5.17 shows the cross-section of the aluminum patterning.

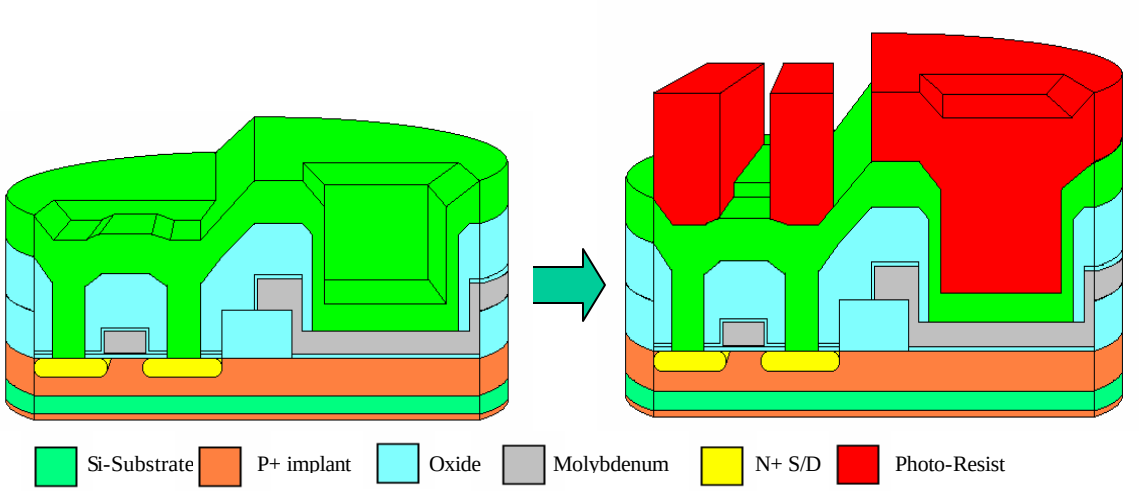

Figure 5.17: Aluminum lithography

Step 25: Aluminum Etch

Aluminum was wet etched using Transene Aluminum Type-A etchant. It was done at 50°C and visually end-pointed. Wafers were then rinsed in DI water for 5 minutes and given a spin-rinse-dry.

Step 26: Resist Strip

Resist was stripped off using solvent strip as described in step 9. The cross-section of device showing aluminum etch and resist strip is shown in Figure 5.18.

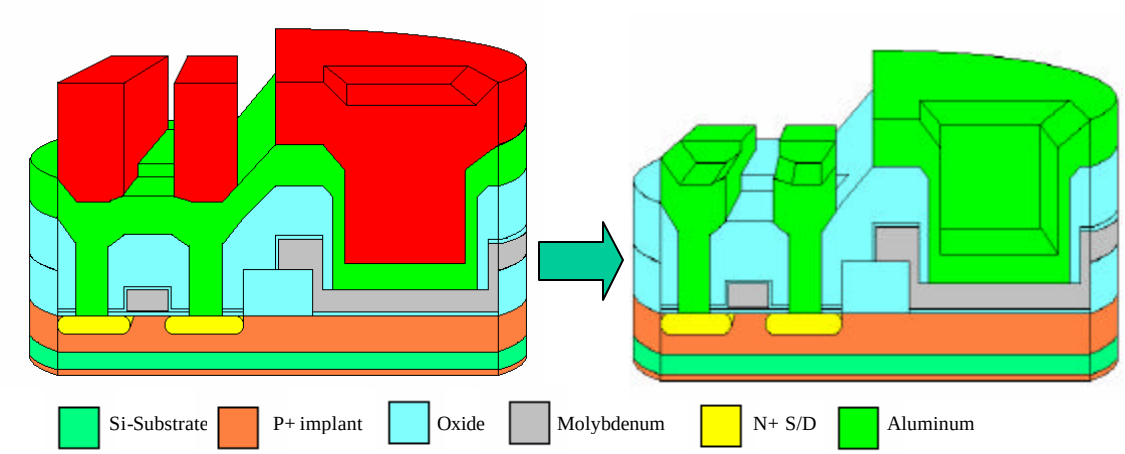

Figure 5.18: Aluminum etch and resist strip

Step 27: Capacitor Lithography

Capacitors were patterned separately in the aluminum to prevent contamination in the aluminum etch bath. If the aluminum for the capacitors were etched at the same time as the transistors, any over-etch would result in molybdenum contamination in the aluminum etch bath. The EAGLEPLG recipe was used with pass 1 to only expose capacitor die. Coat and develop were the same as in step 7. Figure 5.19 shows the capacitor lithography cross-section.

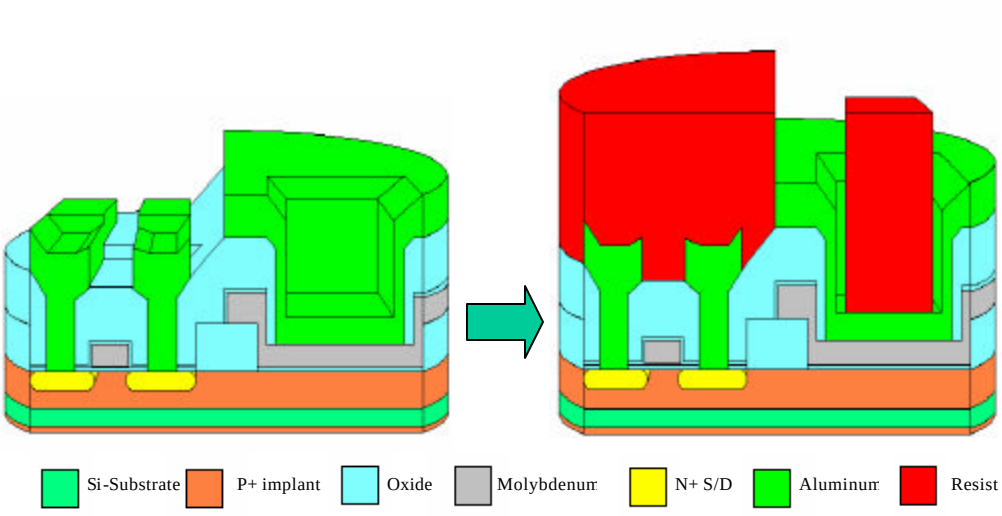

Figure 5.19: Capacitor lithography

Step 28: Aluminum Capacitor Etch

Capacitors were etched with aluminum etchant in pie plates at room temperature. (The etch was not done in the standard bath in order to prevent molybdenum contamination.) The etch took about 10 minutes per wafer. After they were visually end-pointed, they were rinsed with DI water and given a spin-rinse-dry.

Step 29: Resist Strip

Resist was stripped from the wafers as described in step 9. The capacitor etch and resist strip is shown in Figure 4.22.

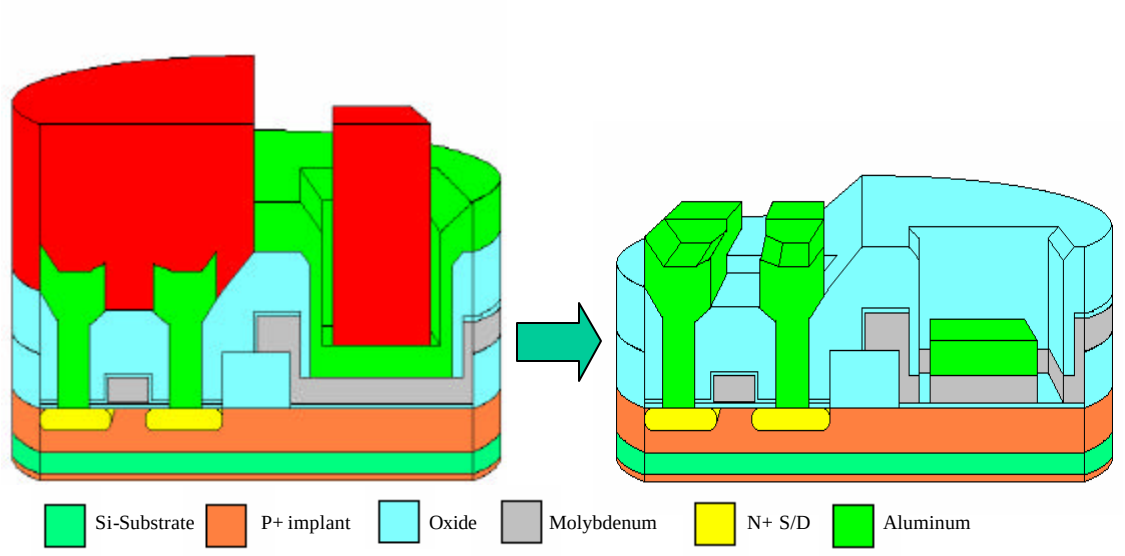

Figure 5.20: Capacitor metal-etch and resist strip.

Step 30: Sinter

An anneal was done at 450°C in H_2N_2 for 30 minutes. At this point the devices were ready to be tested. An enlarged final cross-section of the device is shown in Figure 5.21.

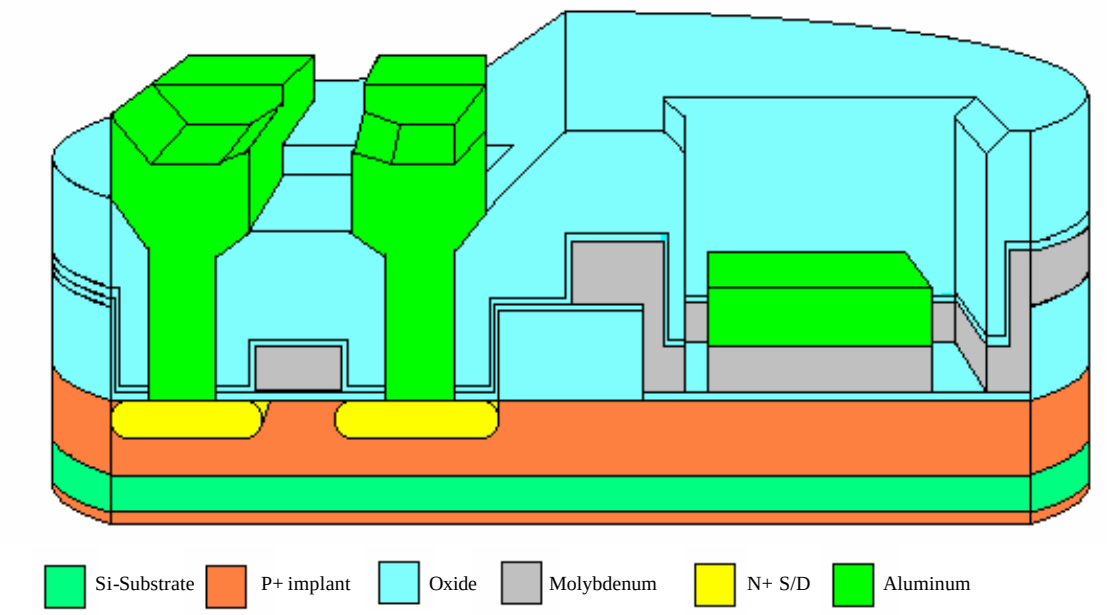

Figure 5.21: Final device cross-section

CHAPTER 6

Capacitance-Voltage Analysis

6.1 Preliminary C-V Results

For the capacitors fabricated as described in Chapter 4, an initial C-V curve was taken for each treatment combination and normalized for comparison purposes. The initial C-V curves are shown in Figure 6.1, with extracted parameters summarized in Table 6.1.

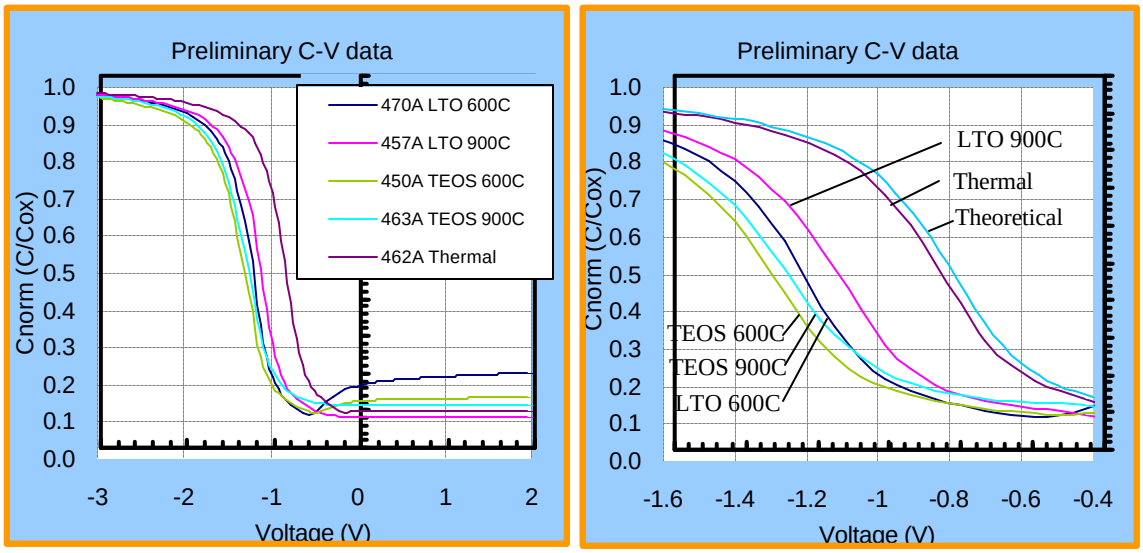

Figure 6.1: Normalized C-V curves

All samples were fabricated on relatively lightly doped p-type silicon, with a boron concentration of approximately $8x10^{14}cm^{-3}$. Note that all samples were sintered in forming gas, 5% H_2 in N_2, at 450°C for 30min. Since a positive charge in the oxide shifts the curve (flatband condition) left, the data supports the hypothesis that annealed TEOS oxides have slightly more total charge than annealed LTO oxides. The thermal oxide has much less total charge, as expected. Annealing the oxides at 900°C appeared to slightly

improve charge levels for the LTO and TEOS oxides when compared to the 600°C annealed samples. Equation 6.1 was used to quantify the total charge in the oxides.

Film	Anneal Temp	Vfb (V)	Qox (/cm^2)
LTO	600°C	-1.26	1.91E+11
LTO	900°C	-1.15	1.39E+11
TEOS	600°C	-1.36	2.26E+11
TEOS	900°C	-1.35	2.16E+11
Thermal	----------	-0.88	-1.27E+09

Table 6.1: Summary of extracted flatband voltage and lumped oxide charge, expressed as an effective interface state density

Equation 6.1: $$Q_{OX} = \frac{C_{ox}\left(f_{MS} - V_{fb}\right)}{q \cdot A}$$

Table 6.1 shows that the total charge for the thermal oxide (expressed as an effective interface state density) appears negative, however the magnitude is less than the precision of the measurement instrument. It is shown in the right of Figure 6.1 that the thermal oxide is actually shifted to the left of the theoretical curve suggesting a slight positive charge. (The theoretical curve was generated using the MDC software with a molybdenum work function of 4.5eV) Most importantly, the charge levels observed for deposited oxides are significantly higher than that of thermal oxide.

The C-V data in Figure 6.1 also shows a unique increase in inversion capacitance for TEOS and LTO deposited oxides annealed at 600°C. Since the oxides deposited are a blanket film on lightly doped p-type silicon, silicon adjacent to capacitors may be inverted from positive oxide and/or interface charge. When measuring the high-frequency capacitance in inversion, this adjacent inversion charge can readily travel to the channel and increase the measured capacitance. While sintering in H_2/N_2 can passivate interface traps with hydrogen, the field inversion charge may be supported by excess hydrogen ions in the bulk oxide resulting from either the combination of silane and oxygen or the dissociation of TEOS. Leftover hydrogen ions can provide a positive

charge, attracting minority carriers (electrons) to the surface in the field regions. This explanation may account for the observed abnormality in inversion-mode capacitance, which is only observed with the TEOS and LTO deposited oxides annealed at the lower temperature. The inversion-mode capacitance on treatment combinations annealed at 900°C appear to have less positive charge, possibly due to desorption of hydrogen at the higher annealing temperature.

After comparing high frequency C-V curves, an initial comparison of interface trap distributions was done using the Kuhn method (described in chapter 3). The results are shown in Figure 6.2.

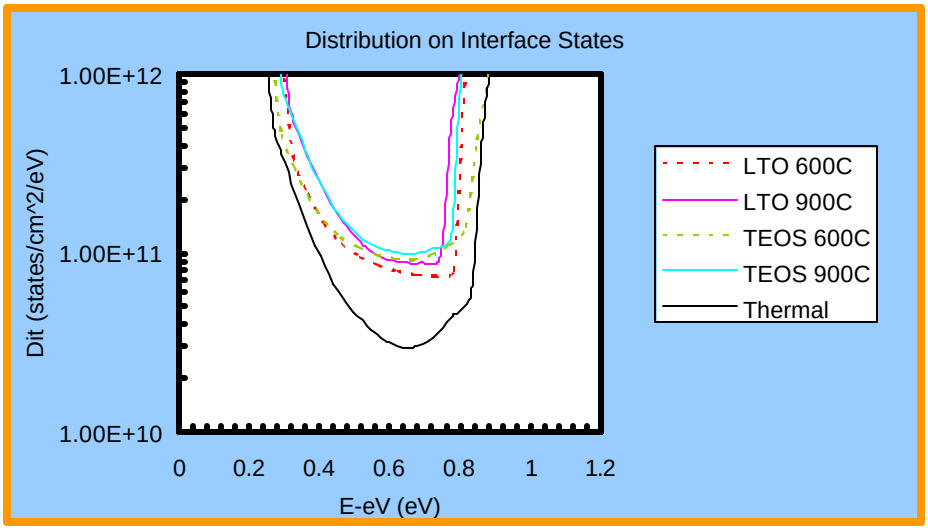

Figure 6.2: Initial interface trap density distributions

The distributions in Figure 6.2 show that the thermal oxide has significantly less interface states around mid-gap compared to that of LTO and TEOS oxides. The mid-gap Dit level for the thermal oxide was around $2x10^{10}$ states/cm^2/eV, while the LTO and TEOS oxides was around $1x10^{11}$ states/cm^2/eV. Interface integrity for the TEOS and LTO oxides did not improve with the 900°C anneal. Considering the accuracy of the measurement, the density of interface traps was roughly the same regardless of the temperature of the N_2 anneal. This is somewhat expected, as it is actually the sinter in H_2/N_2 that is responsible for improving interface states; hydrogen diffuses to the interface and ties up dangling bonds to decrease the number of trap states.

6.2 Mobile Ionic Contamination

The various oxides were tested for mobile ion content (i.e. Na^+, K^+) by means of temperature bias stress testing (TBS) and the triangular voltage sweep (TVS). Figures 6.3-6.5 show results of a TBS tests done on LTO, TEOS and Thermal oxides.

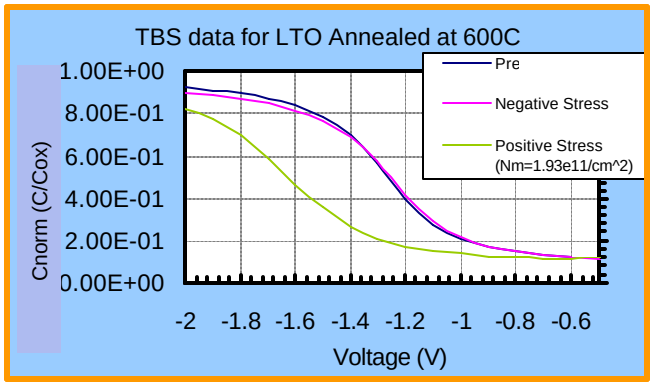

Figure 6.3: TBS plot for LTO oxide annealed at 600°C

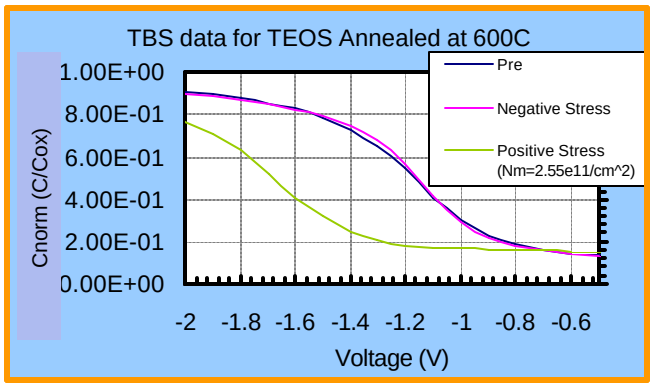

Figure 6.4: TBS plot for TEOS oxide annealed at 600°C

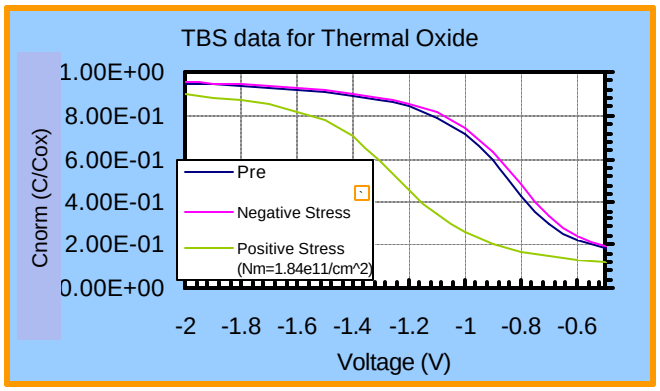

Figure 6.5: TBS plot for thermal oxide annealed at 600°C

TBS measurements were done with a $^{+}$/-3V stress for 10 minutes at 250°C. Based on the voltage shifts observed in Figures 6.3-6.5, mobile ion content was determined to be $1.93x10^{11}$, $2.55x10^{11}$, and $1.84x10^{11}$ ions/cm^2 for the LTO, TEOS and thermal oxides, respectively. Although $N_M \sim 10^{11}cm^{-2}$ for a thermal oxide is significant (source is not certain), there is nearly twice as much mobile charge in the TEOS oxide than with the LTO and thermal oxides. Also note that for all of the TBS Figures, the initial measurement is very close to the measurement after the negative stress. This suggests that the mobile ions initially reside toward the top of the oxide near the gate after fabrication.

TVS sweeps (see section 3.5) were then performed at temperatures between 250-300°C on the various oxides to confirm the trend seen in the TBS measurements. Figure 6.5 below shows a TVS curve for the various oxides performed at 250°C.

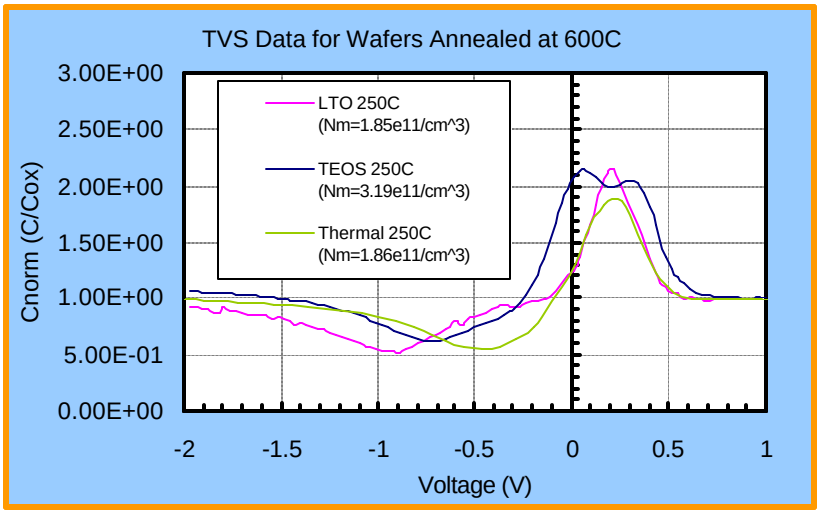

Figure 6.6: TVS curves for wafers annealed at 600°C

For the measurements shown in Figure 6.6, a temperature of 250°C was used with a sweep rate of 0.1V/s. Of the various temperatures and sweep rates implemented, this combination showed the best resolution of the capacitance peaks. When the peaks were

integrated, mobile charges of $1.85x10^{11}$, $3.19x10^{11}$ and $1.86x10^{11}$ ions/cm^2 were calculated for the LTO, TEOS and thermal oxides. Like the TBS data, the TVS data showed that the TEOS oxide had much more mobile ionic charge than the LTO and thermal oxides did. Values determined by the different methods were also similar, showing consistency between the measurement techniques.

In addition to determining mobile ion content (cumulative amount), the TVS test showed two peaks for the TEOS oxide (see Figure 6.5). Although it may be subtle, the two peaks indicate there are more than one species of ionic contamination in the PECVD TEOS deposited film. TVS measurements were also taken on wafers annealed at 900°C. Results are shown in Figure 6.7 and summarized below in Table 6.2.

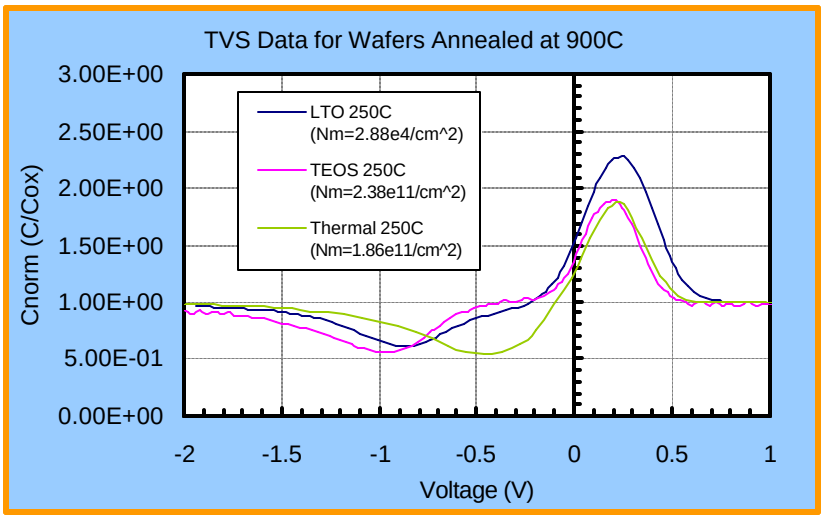

Figure 6.7: TVS data for wafers annealed at 900°C

Temp.	LTO 600C	TEOS 600C	LTO 900C	TEOS 900C	Thermal
250C	$1.85Ex10^{11}$	$3.19x10^{11}$	$2.88x10^{11}$	$2.38x10^{11}$	$1.86x10^{11}$
275C	$1.91x10^{11}$	$4.63x10^{11}$	$3.13x10^{11}$	$2.43x10^{11}$	$1.87x10^{11}$
300C	$1.95x10^{11}$	*	$3.54x10^{11}$	$2.53x10^{11}$	$1.76x10^{11}$
Average	$1.90x10^{11}$	$3.91x10^{11}$	$3.18x10^{11}$	$2.45x10^{11}$	$1.83x10^{11}$

Table 6.2: TVS Measurement Summary - all measurements in ions/cm^2

* sample measurements not reasonable due to leakage current

Measurements summarized in Table 6.2 suggest that the higher temperature anneal is successful in reducing the measurable mobile charge for the TEOS-oxide. It is possible that the higher temperature allows for the mobile charge to become trapped near the gate. Note that there were not multiple peaks observed in the TEOS-oxide that was annealed at 900°C; the anneal effectively removes the influence of one contaminant but not the other. To further investigate this, a TEOS-oxide with no anneal was measured to confirm the existence of multiple contaminants. Results are shown in Figure 6.8 below.

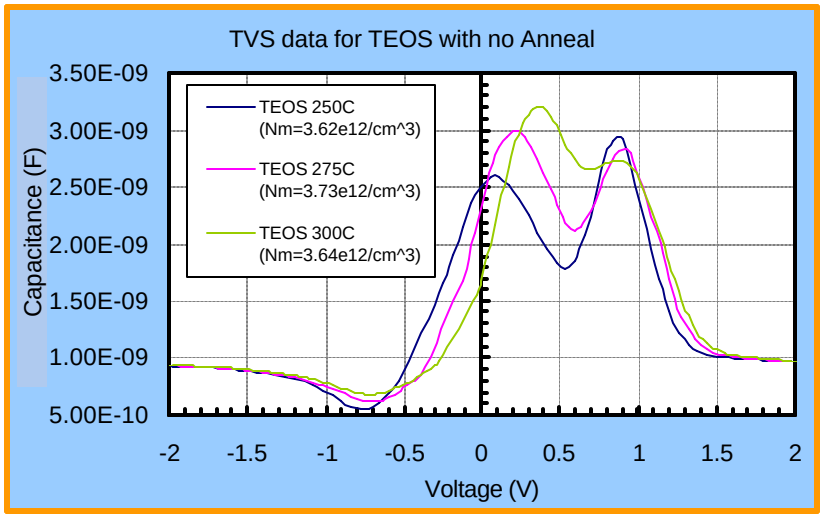

Figure 6.8: TVS of TEOS with no anneal

The TVS curves exhibit very distinct peaks showing that there are definitely two mobile ionic species present. The peak on the right is thinner and higher than the one on the left, especially at lower temperatures. It also is shifted further to the right on the voltage scale, meaning that it is repelled from the other charge sooner than the other species. Because of this, it can be inferred that the ion causing the right peak has a lower mass and is more mobile (see section 3.5 for TVS theory).

Figure 6.8 shows that the anneal is gettering or trapping a significant portion of mobile charge. The measurements in Figure 6.7 show a calculated mobile charge of ~3.65×10^{12} ions/cm^2. This is an entire order of magnitude higher than measurements done on TEOS receiving the 600°C anneal. To gain a better insight as to which peak is removed at higher temperatures, the TEOS-oxide device which received no anneal was plotted with the wafers that were annealed at 900°C; the results are shown in Figure 6.9.

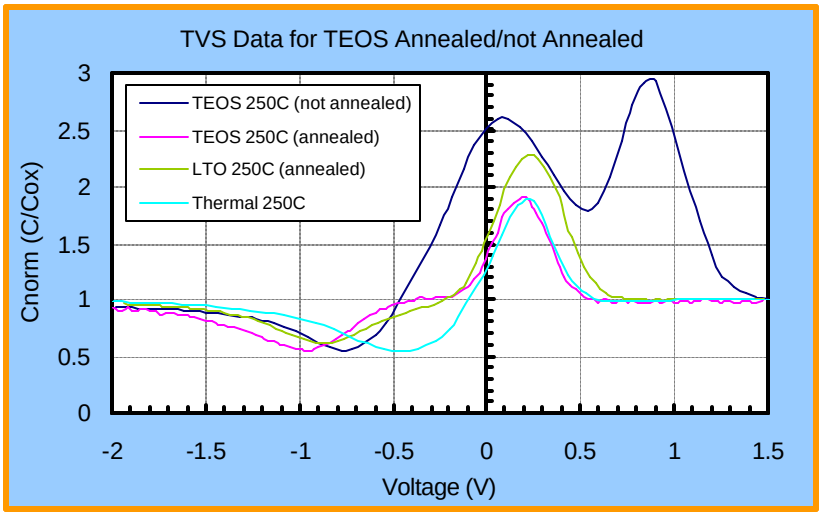

Figure 6.9: TVS of TEOS-oxide on both non-annealed and annealed capacitors

Figure 6.8 shows that the peak on the right appears to be removed from the anneal. This is the peak corresponding to the ion with less mass that is more mobile. Because it is more mobile, it appears to diffuse and segregate to trapping sights during the annealing process.

It is also worth noting that mobile ion content was also investigated for an LTO oxide that was not annealed. This film did not show any noticeable difference than the LTO oxide annealed at 600°C. Mobile charge levels were around 2×10^{11} ions/cm^2.

6.3 Stress-Induced Defects Resulting from TBS

When doing a temperature bias stress test it was noticed that the high frequency C-V curve became elongated after the stress, suggesting that interface traps had been created during the stressing. Under aggressive TBS conditions (300°C, >2MV/cm, 10min), a high electric field is dropped across the oxide at an elevated temperature. With elevated temperatures and a high electric field, weak bonds at the interface begin to break and create interface states. This mechanism of damage is strikingly similar to damage induced by exposure to plasma. With this similarity in mind, capacitors were stressed by inducing high electric fields at elevated temperatures. In doing so, valuable insight was gained regarding the different oxides and their susceptibilities to interfacial damage.

6.3.1 TBS on Oxides Annealed at 600°C

To investigate susceptibilities of the various oxides to interface degradation, C-V curves were taken before and after a 10V stress for 10minutes at 300°C. Figure 6.10 shows the results. After stressing the films at elevated temperatures, the redistribution of mobile ions within the oxide causes a shift in the C-V curve. To clarify and best present the induced interfacial damage, the post-stress C-V curves were shifted back and placed directly over the initial measurements. From looking at the plot, it is evident that the TEOS-oxide undergoes the highest degree of stretching from the stress. LTO and Thermal oxides showed minor stretching that was significantly lower than that of the TEOS-oxide.

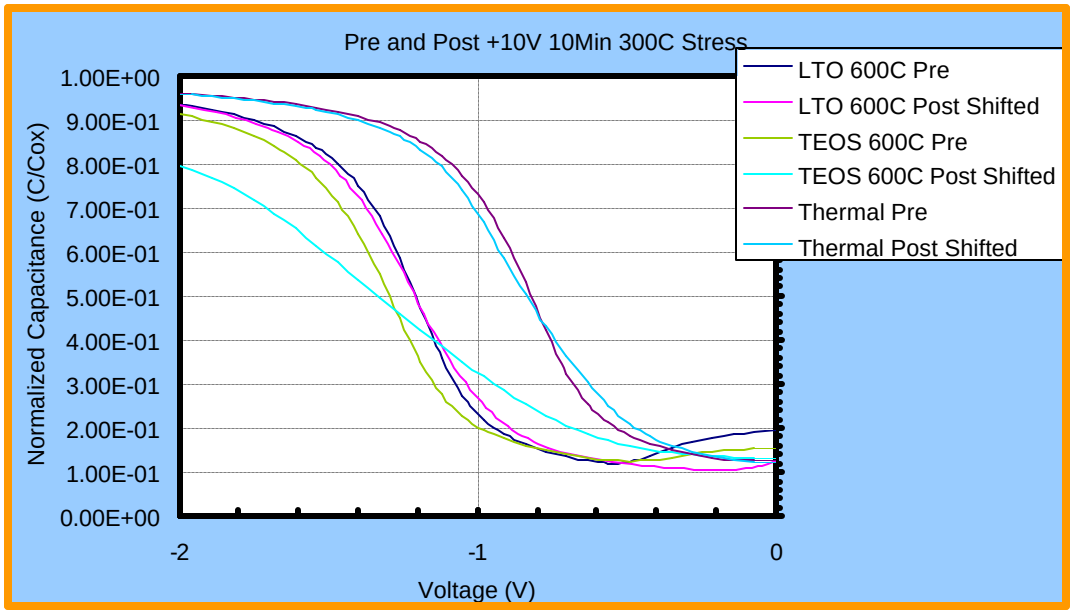

Figure 6.10: C-V curves before and after stressing oxides annealed at 600°C

To compare the severe stretching of the TEOS oxide to the LTO and thermal oxide numerically, the maximum slope of the C-V curves were taken before and after the stress. The differences between these two values are graphed in Figure 6.11.

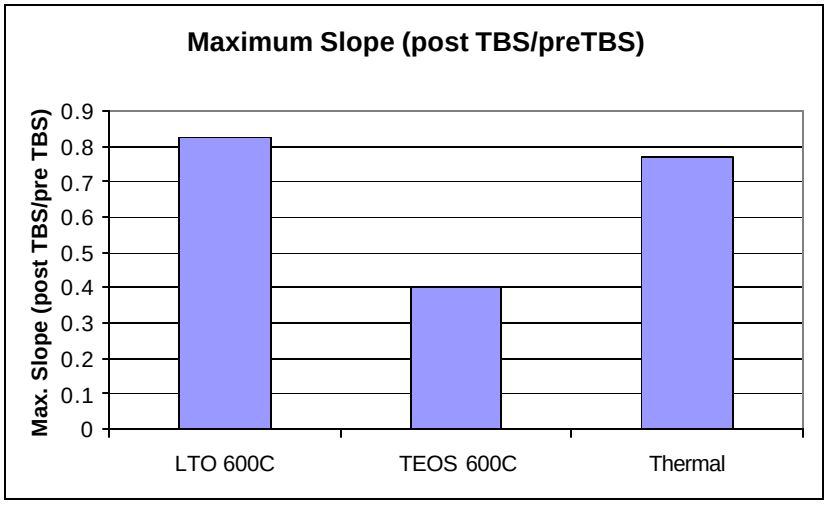

Figure 6.11: Decrease in maximum C-V slope for 600°C oxides

A decrease in maximum slope is a way of showing stretching caused by interface trap states. When numerically plotted, the slope decrease is significantly greater for the TEOS oxide

meaning that far more interface states are created in the TEOS oxide than the LTO and thermal oxides when a stress is applied. In Figure 6.11, a value of one corresponds to the optimal situation where no stretching results from the stress. A value of zero corresponds to a worst-case scenario where the C-V curve stays flat and doesn't even invert after the stress is applied. Differences between damage observed in the thermal and LTO oxides do not appear to be significant. This minute aberration could be from something as trivial as a fluctuation in surface doping.

6.3.2 TBS on Oxides Annealed at 900°C

Similar tests were performed on the oxides annealed at 900°C, however both positive and negative 10V stress (~2MV/cm) were used to exaggerate stretching of the C-V curves. Figure 6.12 shows the curves before and after the induced stress.

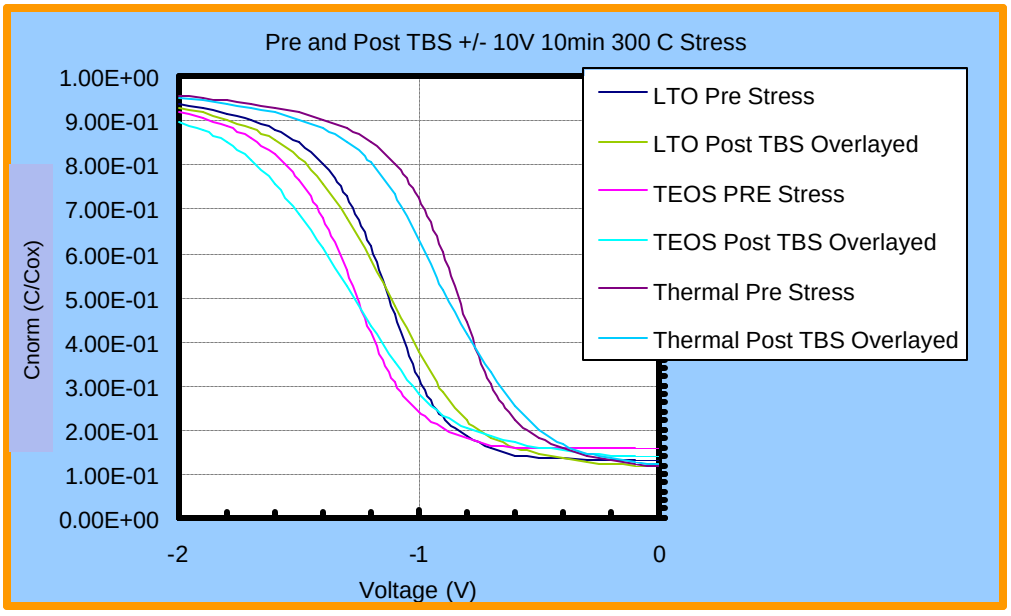

Figure 6.12: C-V curves before and after stressing oxides annealed at 900°C

All of the oxides annealed at 900°C showed very similar degree of distortion in the C-V curve after exposure to stress. It shows that when the TEOS film is annealed at a higher temperature, it behaves much more like the LTO and thermal oxides. On the TEOS-oxide sample, the susceptibility to interface state generation appears to be significantly reduced with the higher temperature anneal, however this improvement is not apparent on the LTO and thermal oxide samples. Figure 6.13 quantifies the stretching of the C-V characteristics over the measured samples for comparison. The LTO sample that was annealed at 900°C appears to stretch more in response to TBS than the 600°C annealed sample, however it must be noted that the TBS on 900°C annealed samples was done under both positive and negative applied bias. These results indicate that the nature of the oxide-silicon interface has become increasingly similar for the samples annealed at 900°C.

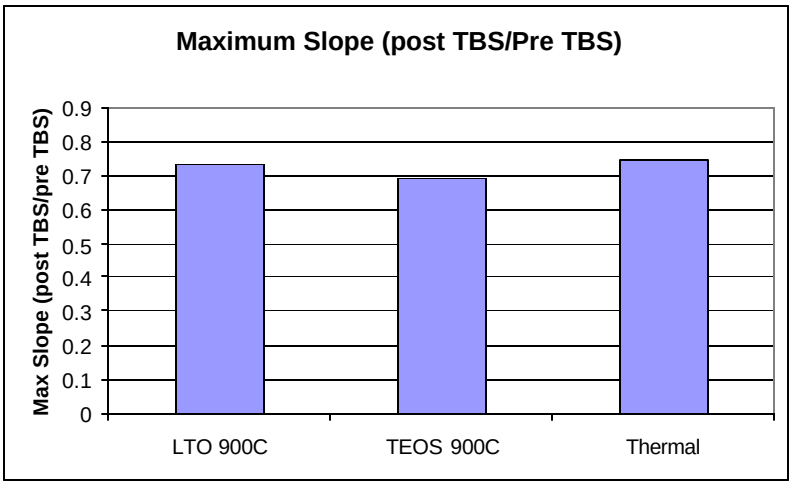

Figure 6.13: Decrease in maximum C-V slope for 900°C annealed oxides

6.3.3 Interface Trap Densities

To show that the stretching in the C-V curves was caused by induced interface states, Interface trap density distributions were taken before and after the stress tests for each oxide type. Figures 6.14, 6.15 and 6.16 show that the main change in trap distribution occurs near mid-gap. This shows that the stress actually broke bonds at the oxide-silicon interface for all of the oxides studied.

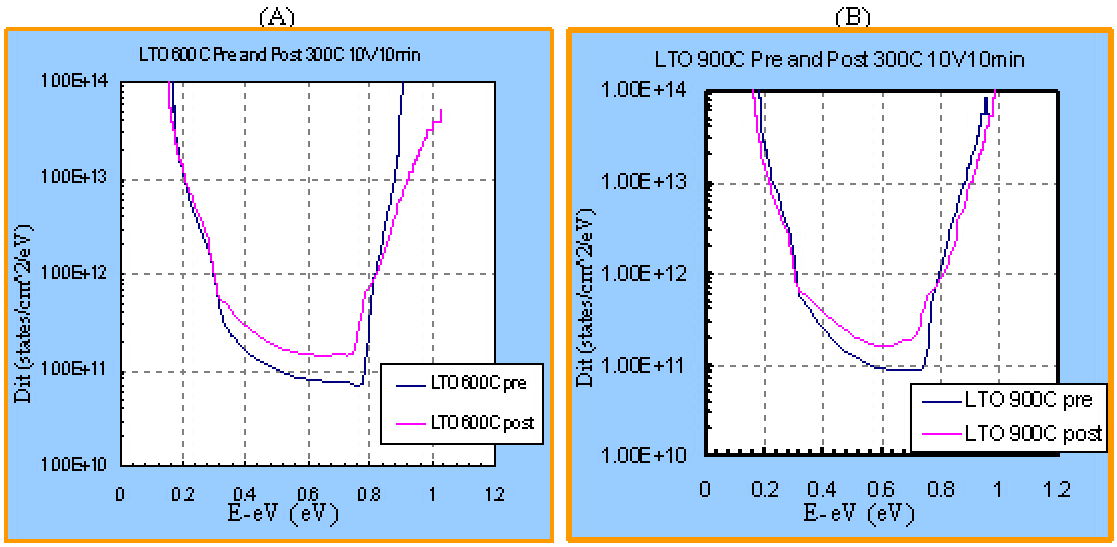

Figure 6.14: LTO-oxide D_{IT} before and after stress

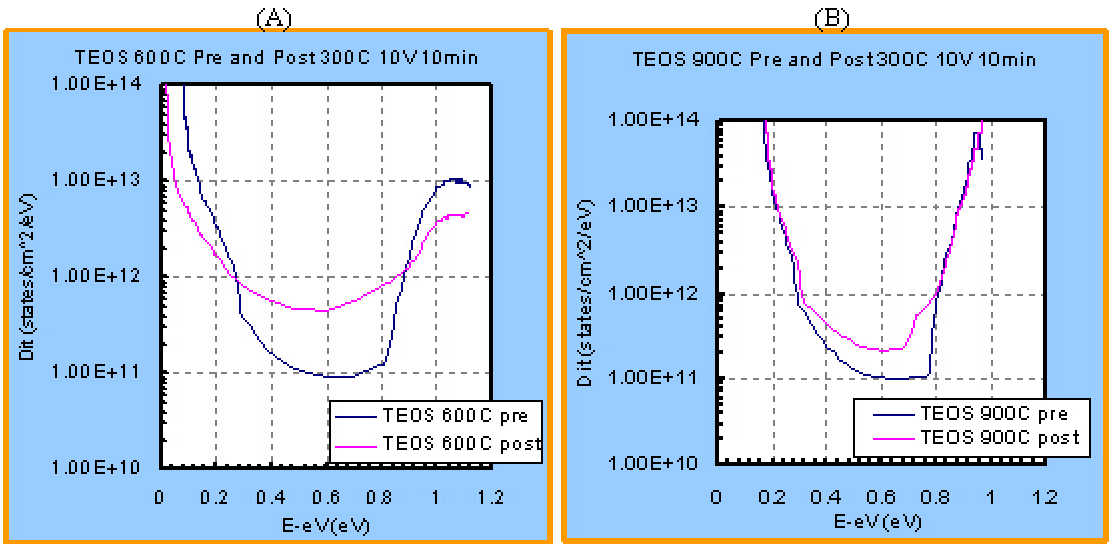

Figure 6.15: TEOS-oxide D_{IT} before and after stress

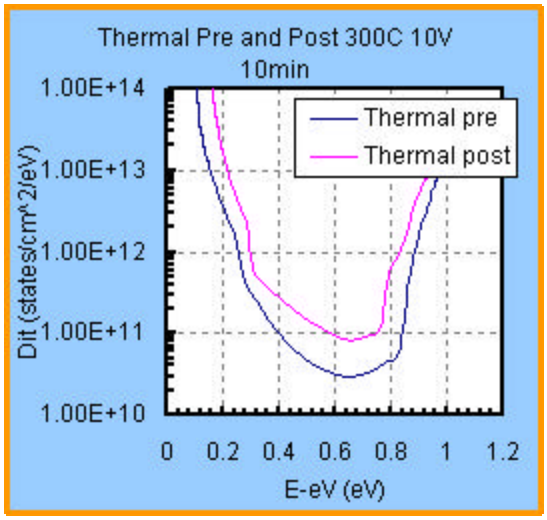

Figure 6.16: Thermal oxide D_{IT} before and after stress

Figures 6.14, 6.15 and 6.16 show that there was, in fact, an increase in interface trap density. In all Figures, the major increase in interface trap density occurs near mid-gap. As suggested by the stretching of the high frequency C-V curves, the TEOS oxide annealed at 600°C suffered the most interface state generation when exposed to the stress,

as shown in Figure 6.14(A). In order to compare the extent of the damage created at the interface, Dit was taken at mid-gap before and after the applied stress for all of the films. The results are shown in Figure 6.17 below.

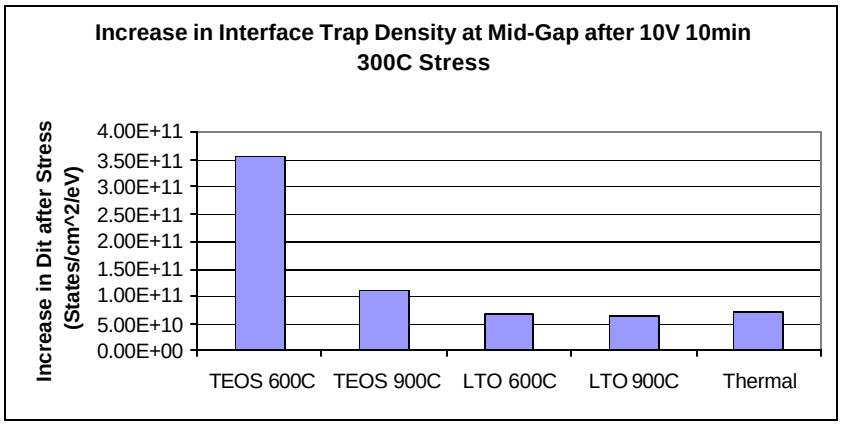

Figure 6.17: Increase in Dit after applied stress for TEOS, LTO and thermal oxides

6.4 Breakdown and Leakage Current Measurements

Breakdown and leakage current measurements were taken on the initial capacitors annealed at 600°C. This was done in order to predict the susceptibility to bulk trapping during plasma processing. If a film has significant leakage, it will be more likely to undergo bulk charging during plasma processing [25]. Of many measurements taken, Figure 6.18 shows typical breakdown plots of the various oxides. Applied bias conditions were negative, placing the device in accumulation rather than inversion and minimizing the resulting voltage drop across the semiconductor surface region. Figure 6.18 shows the absolute value of the voltages and currents from the measurements.

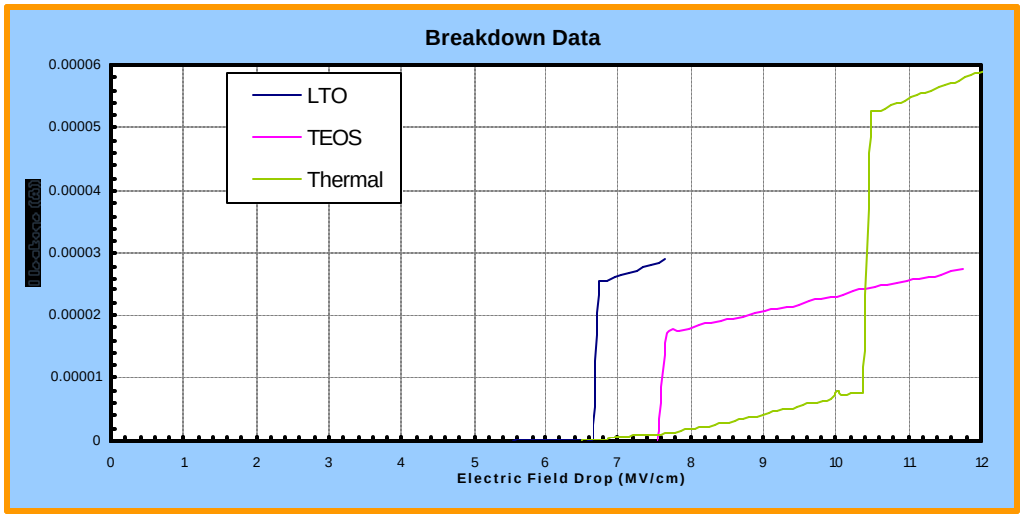

Figure 6.18: Breakdown plots of LTO, TEOS and thermal oxides

Average breakdown fields were 10.68MV/cm, 8.13MV/cm and 6.98MV/cm for the thermal oxide, TEOS oxide and LTO oxide, respectively. Despite leakage current prior to breakdown, the thermal oxide was much more resistant to the induced high field. When these measurements were taken, the leakage currents were also recorded. Figure 6.19 shows leakage currents for the various films at both 2MV/cm and 4MV/cm.

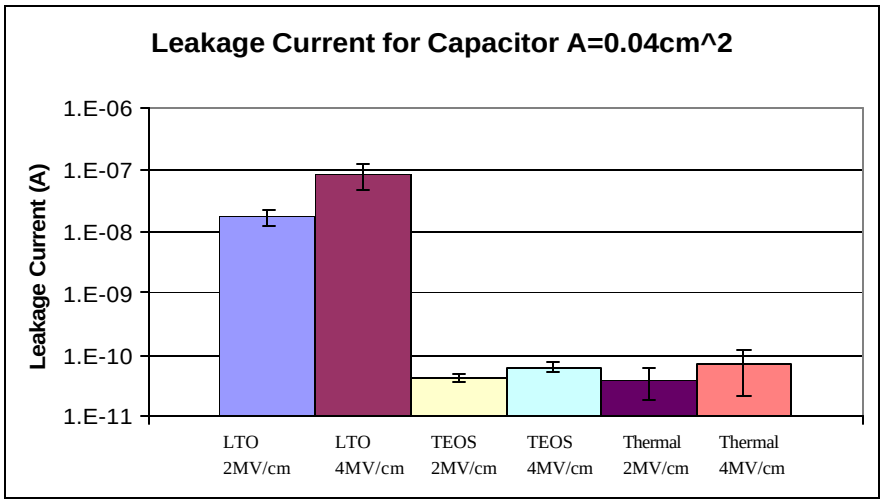

Figure 6.19: Leakage currents of LTO, TEOS and thermal oxides with 1s error bars

The leakage currents of the LTO oxide were unexpectedly high when compared to the TEOS and thermal oxides. The LTO oxide had much higher leakage currents, which indicated that it may be more susceptible to bulk charging during high-field plasma processing than the TEOS and thermal oxides.

6.5 Conclusions from C-V Characterization

Based on TBS testing and leakage currents observed in the initial capacitor study, it can be anticipated that all three oxides will react somewhat differently to plasma exposure during transistor fabrication. The TEOS oxide will most likely suffer the highest degree of interface degradation, especially when only annealed at 600°C. Severe stretching of the C-V curves and Dit measurements before and after stress suggest this. Mobile charge measurements show that the un-annealed TEOS will be nearly an order of magnitude higher in charge than the LTO and thermal oxides. A 900°C anneal should remove the majority of the induced damage making it more comparable to the degree of damage observed with the LTO and thermal oxides. The very low leakage current measurements suggest that bulk oxide charging will be minimal and comparable to that of the thermal oxide.

The LTO oxide may suffer a significantly higher degree of bulk trapping during high field plasma processing, as indicated by significantly higher leakage current. As a result, threshold voltages are expected to be significantly higher than those fabricated with TEOS and thermal gate oxides. Slight interfacial damage is expected with the LTO gate oxide at both annealing temperatures. This could cause slight distortion in C-V and I-V

curves. The degree of interfacial damage should be far less than that of the TEOS when they are annealed at the lower temperature.

The thermal oxide should present the best-case situation with respect to both interface damage and bulk charge effects. This is supported by minor changes in C-V characteristics observed during TBS testing and low leakage current levels at high applied bias conditions.

Chapter 7

INVESTIGATION ON INTEGRATED DEVICES

7.1 Integrated Capacitors

The capacitors exposed to the full transistor fabrication process were studied to determine whether or not process induced damage was present in the various gate oxides. Stretching of the C-V curves was used to qualitatively determine which treatment combinations underwent interfacial damage during the transistor fabrication. Figures 7.1, 7.2 and 7.3 show C-V plots for capacitors fabricated with LTO oxide, TEOS oxide and thermal oxide.

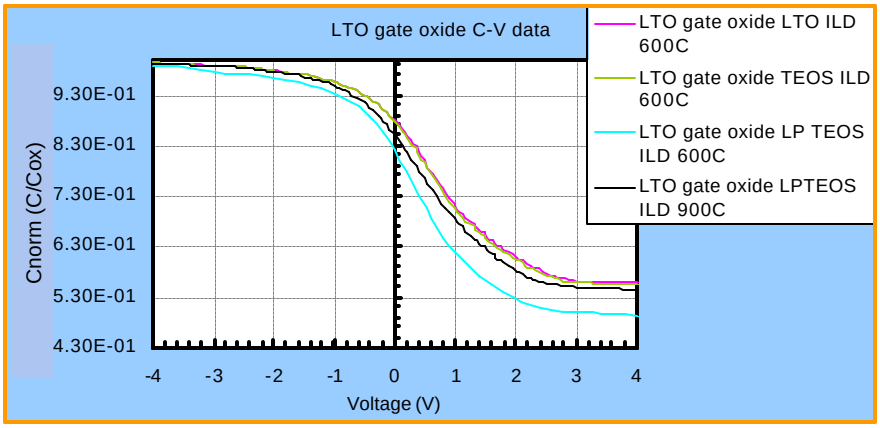

Figure 7.1: C-V curves of integrated LTO-Oxide capacitors

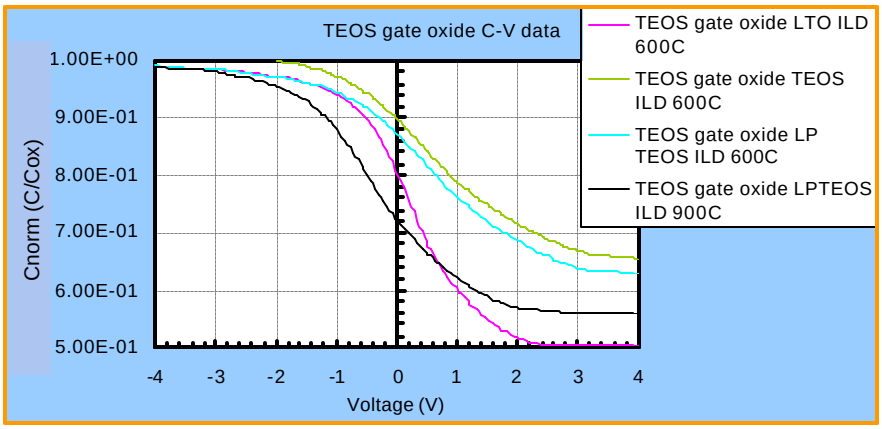

Figure 7.2: C-V curves of integrated TEOS-oxide capacitors

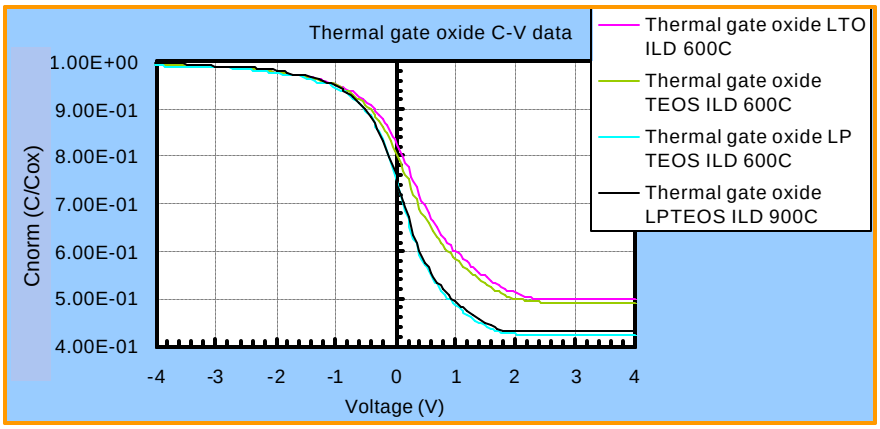

Figure 7.3: C-V curves of integrated thermal oxide capacitors

Despite being normalized, inversion capacitances vary between treatment combinations. This is most likely a result of doping non-uniformity observed in the p-well doping concentration (discussed further in the next section).

For the LTO gate oxides, Figure 7.1 shows that exposure to plasma during the ILD deposition did not appear to significantly alter the shape of the C-V curve. The degree of stretching is very similar to that of the reference wafer, which used LTO oxide as the ILD.

As predicted by the preliminary capacitor study, significant stretching of the C-V curve resulted for all PECVD-TEOS gate oxide capacitors exposed to the plasma in the ILD deposition. Figure 7.2 shows far less stretching when the LTO ILD is used. This provided evidence that it was, in fact, the exposure to plasma in the ILD deposition that induced the damage. As suggested by initial capacitor data, some of the induced damage appeared to be annealed at 900°C; the C-V curve of this treatment combination was noticeably steeper than those annealed at 600°C.

No visible stretching from the creation of interface states was observed in the thermal gate oxide C-V curves. Figure 7.3 actually shows a steeper C-V curve for wafers processed with the low power (LP, 50W) TEOS ILD. It may be the case that interface states are actually reduced, resulting in a compression rather than a stretching of the C-V curve.

The lack of shifting or distortion of thermal gate oxide C-V characteristics supports the interpretation that the thermal oxide devices are not as susceptible to plasma-induced charge. However, it must be noted that the capacitors have an enormous surface area compared to the transistors they were processed with. As a result, they collect less charge per area compared to transistor gates, and drop less electric field across the oxide during plasma processing. Thus, the influence of a plasma process may be different on transistor structures that are exposed to higher fields during the plasma deposition process. The investigation on transistor structures will be discussed over the remainder of this chapter.

7.2 Reference Wafers with LTO ILD

The reference wafers were analyzed first in order to show that damages observed throughout the experiment are a direct result of the ILD deposition. Current-Voltage (I-V) characteristics in both the linear and saturation mode of operation are shown in Figures 7.4 and 7.5.

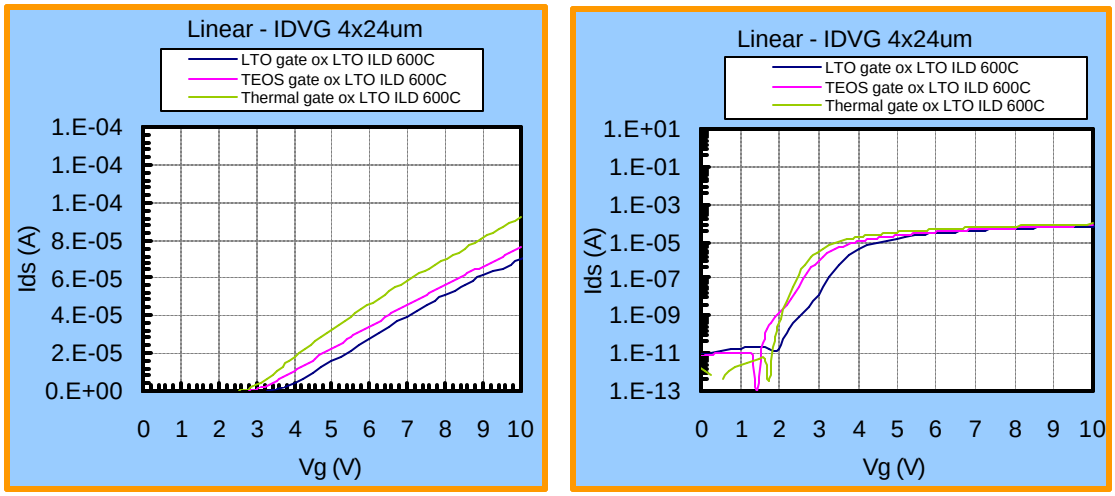

Figure 7.4: Linear I_D-V_G curves for devices with LTO ILD (V_D=0.1V). The channel dimensions are 4µm x 24µm for the length (L) and width (W), respectively

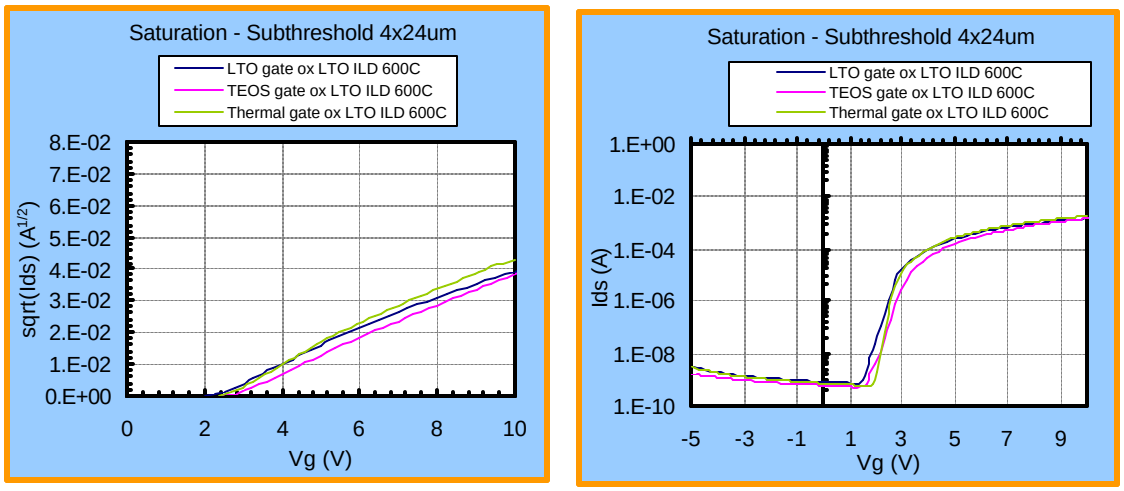

Figure 7.5: Saturation I_D-V_G curves for devices with LTO ILD (V_D=10V)

For all I_D-V_G Figures, the left plot shows the current on a linear scale and the right plot shows the current on a log scale. The linear scale is useful in extracting the threshold voltage. The threshold voltage is taken where the maximum slope portion of the characteristic extrapolates to the x-axis. The plot with the current on the log scale is useful in comparing sub-threshold swing and stretching from interface states which are operative at gate bias below threshold. As interface trap states fill and empty, the current response to gate bias is disrupted resulting in a stretching of the I-V curve. Also, all results shown in this chapter are representative of trends that were verified at several transistor sizes among different die.

Figures 7.4 and 7.5 show threshold voltages are within 1-2 volts of each other for the various gate oxides. Although this variation appears quite high, the values are consistent with the confidence limits of the well doping *. The plots on a log scale show that off-state leakage currents are very similar for all of the reference samples. There are,

* Further analysis confirmed that the well drive-in added a significant amount of boron to the device wafers, thus raising the threshold voltage and inducing significant variation across the wafer.

however, minor variations in shape of the I-V curves when observed on the log scale. Specifically, there is a small kink in the I-V curves taken with TEOS and LTO gate oxides. These could be a result of minor interface damage induced during the gate etch or metal deposition plasma processes.

It is also worth mentioning the discontinuities observed at low current levels; these are simply a result of noise in the measurement. Negative currents are sometimes recorded when current levels are below the measurement capabilities of the tool. In these instances, it is necessary to use the absolute value in order to show the continuous plot on a log scale.

Although there are minor variations in the I-V curves for the different gate oxides, they serve as an adequate control group. Experiments that investigate the influence of the plasma ILD process show differences that are significantly higher than this source of unintentional variation.

7.3 Standard TEOS ILD Annealed at 600°C

The effects from the standard TEOS (205W) ILD deposition process were then analyzed for the different gate oxides. I-V curves are shown in the following Figures.

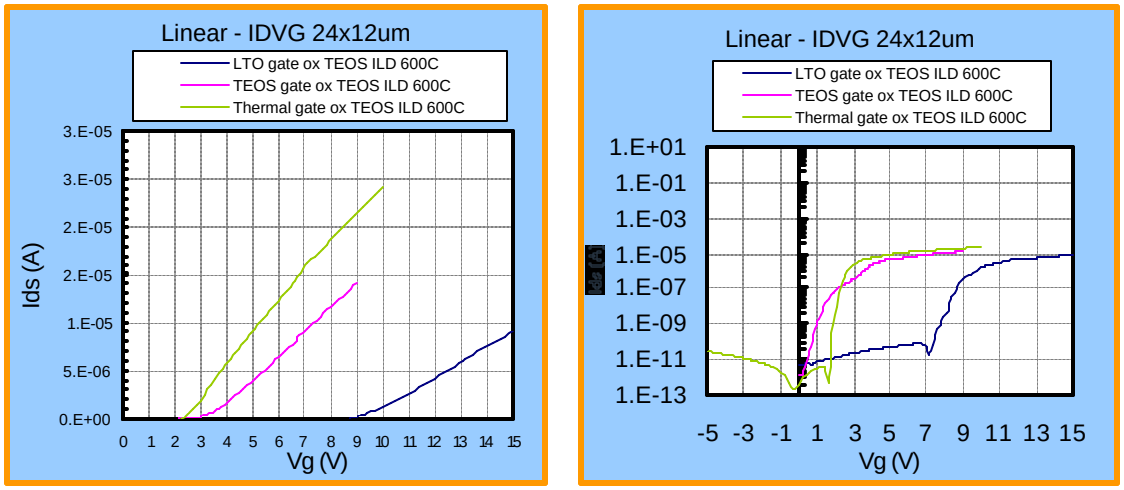

Figure 7.6: Linear I_D-V_G curves for devices with std. TEOS ILD (V_D=0.1V)

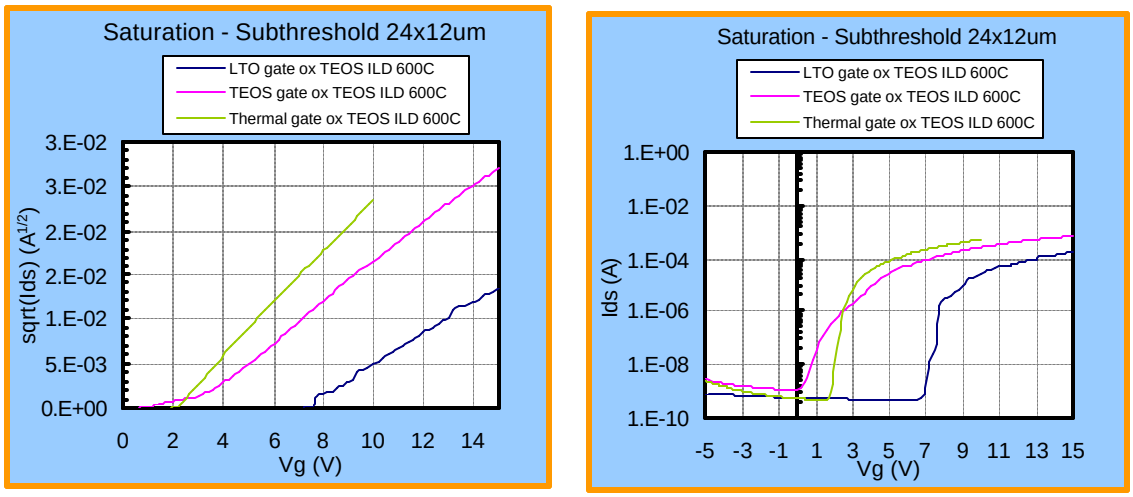

Figure 7.7: Saturation I_D-V_G curves for devices with std. TEOS ILD (V_D=10V)

As suggested by C-V analysis, the TEOS gate oxide showed a significant degree of stretching in the I-V curve from exposure to the ILD plasma. The influence of interfacial traps were significantly more pronounced in the TEOS gate oxide than with the LTO and thermal oxides, in agreement with the assessment C-V measurements taken before and after temperature bias stress. The average sub-threshold swing was extracted for each treatment combination and plotted to quantitatively show that the TEOS gate oxide suffered the most interfacial damage from the TEOS ILD deposition. For consistency, this slope was taken at the low-current range (best-case region) of the curve each time. The results are shown in Figure 7.8.

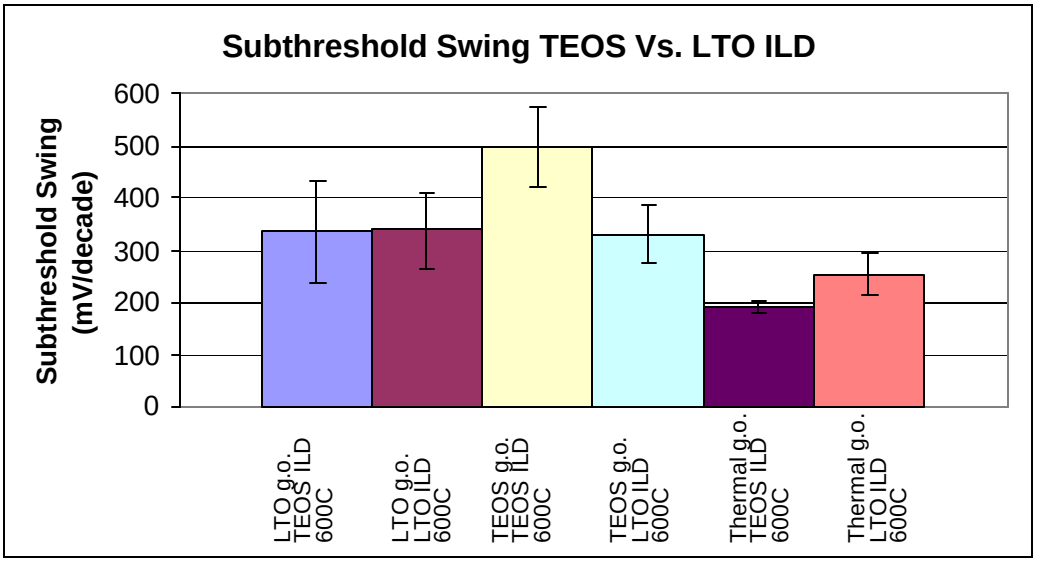

Figure 7.8: Sub-threshold swing for devices w/ TEOS & LTO ILDs and 1s error bars

Figure 7.8 shows that sub-threshold slopes appeared to actually improve for thermal oxides receiving a TEOS ILD. This also agrees with data presented in Figure 7.3, showing an increase in the slope of the C-V curves for thermal oxides receiving TEOS ILD depositions. The resulting change in the interface state distribution of the thermal oxide appears to have caused a compression of the electrical curves rather than a stretching. A plausible explanation as to why this happened involves hydrogen passivation; unreacted hydrogen from dissociated TEOS may be tying up dangling bonds during the ILD process, causing it to behave as a sintering process. Significant differences in oxide charge (shown in Table 6.1) may explain why this improvement is not apparent on the deposited oxides.

A prominent increase (right-shift) in threshold voltage is observed with the LTO gate oxide (Figure 7.6-7.7). The threshold voltage shift was over six volts. Although the non-uniformity of the well doping may account for up to 2V uncertainty (worst-case) in the threshold voltage, the observed voltage shift appears to be a significant response of the

treatment combination. This suggests that charge was injected into the bulk LTO gate oxide during the ILD deposition; bulk electron trapping resulted in a large negative oxide charge, causing the threshold voltage to right-shift dramatically. The very high leakage currents measured in the LTO capacitors (see section 6.3) suggested a susceptibility to bulk charging during plasma processing. This explanation of the observed threshold voltage shift is consistent with the original assessment on capacitor structures.

Note that the I-V curves for the transistors containing LTO gate oxides were not as smooth as those from TEOS-oxide and thermal oxide devices. This did not appear to be error in the measurement; bias conditions were swept many times at various speeds resulting in the same curve. The observed jaggedness may be a result of field-induced trap release as the devices were measured.

7.4 Standard TEOS ILD Annealed at 900°C

Unfortunately treatment combinations containing the standard TEOS ILD recipe that were annealed at 900°C did not yield working devices. The molybdenum gates oxidized during the anneal causing failure in all of these devices. Figure 7.9 shows a working device (different treatment combination) and one that was oxidized during the high temperature anneal.

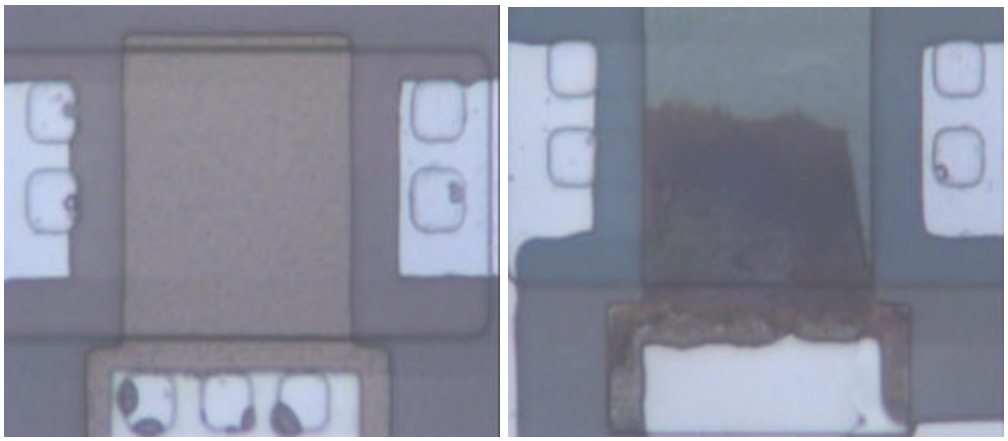

Figure 7.9: Oxidation of the Molybdenum Gate. The picture on the left side of Figure 7.6 shows a working device that was not oxidized. On the right is a device that was oxidized, showing an obvious discoloration halfway up the gate.

The wafers that received the low power TEOS (50W) ILD recipe did not oxidize in the 900°C anneal, which suggests that the resulting film provided a better diffusion barrier against oxygen. This may have prevented residual oxygen in the furnace ambient from reaching the molybdenum layer during the anneal.

7.5 Low Power TEOS ILD Annealed at 600°C

The goal of using the low power TEOS ILD (50W, decreased from 205W) was to lower the electric field dropped across the gate oxide during the deposition. A lower resulting electric field supports a significantly less tunneling current into the gate oxide, and thus translates to less bulk oxide charge trapping. This would also support less interfacial damage and interface states. Figures 7.10 and 7.11 show the I-V curves from wafers with a low power TEOS ILD that were annealed at 600°C.

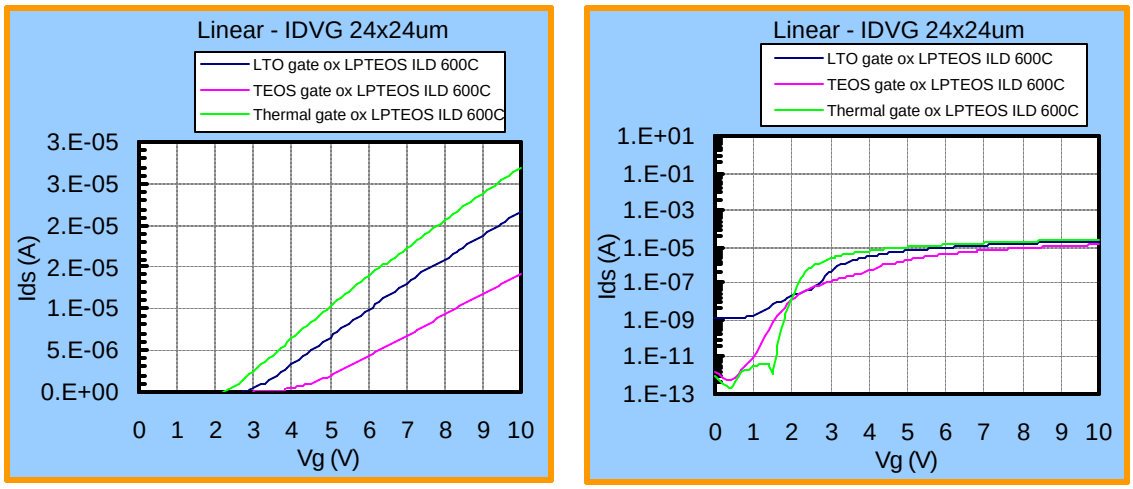

Figure 7.10: Linear I_D-V_G curves for devices with low power TEOS ILD (V_D=0.1V)

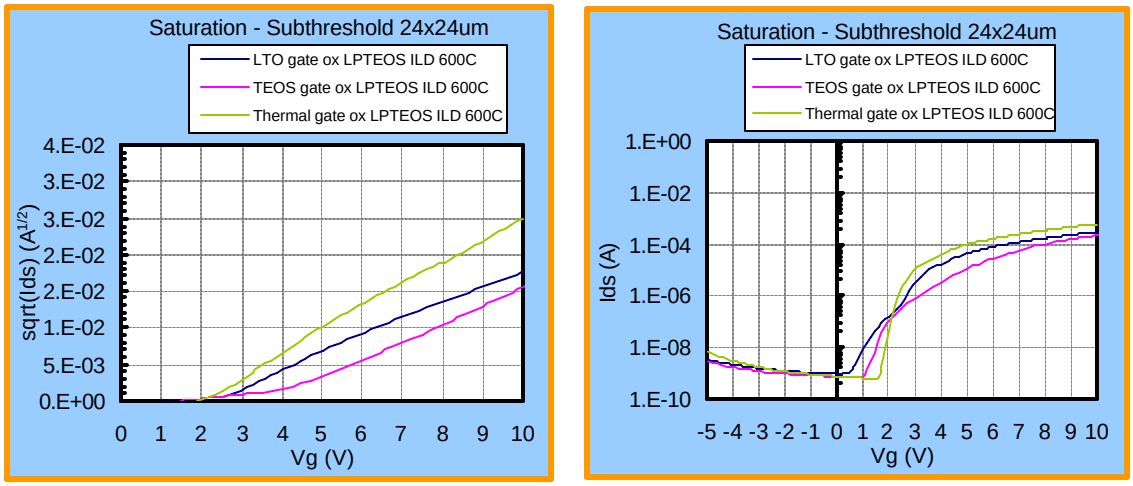

Figure 7.11: Saturation I_D-V_G curves for devices with low power TEOS ILD (V_D=10V)

The TEOS ILD with a lower deposition power resulted in significantly less bulk charge trapping, presumably due to a lower level of tunneling current. Unlike results on devices that received the standard TEOS ILD recipe, there was no dramatic increase in threshold voltage for transistors with LTO gate oxides.

However, the plots in Figures 7.10 & 7.11 show that there is significantly higher influence of interface states on the LTO and TEOS gate oxides compared to those

fabricated with the standard ILD recipe. This is observed through the stretching of the I-V curves seen quite clearly on the log-scale plots. There are also kinks in the characteristics that are more pronounced than they are with the standard TEOS ILD recipe. This suggests that the creation of interface trap states is more significant when the TEOS ILD is deposited at a lower power; a counter-intuitive assessment. The most probable reason for this is that the deposition times required for the low power ILD were more than three times greater than those deposited with the standard recipe. Wafers that received the standard TEOS recipe were exposed to the plasma for only 30 seconds, while the wafers getting the low power recipe were exposed to the plasma for 100 seconds. This implies that there may be a tradeoff between the deposition power and the nature of resulting oxide and/or interface charge states created. Higher deposition power results in more bulk oxide trapping, while lower power results in more interfacial degradation. To quantify this phenomenon, average sub-threshold slopes of these wafers were plotted with those of the reference samples, with results shown in Figure 7.12.

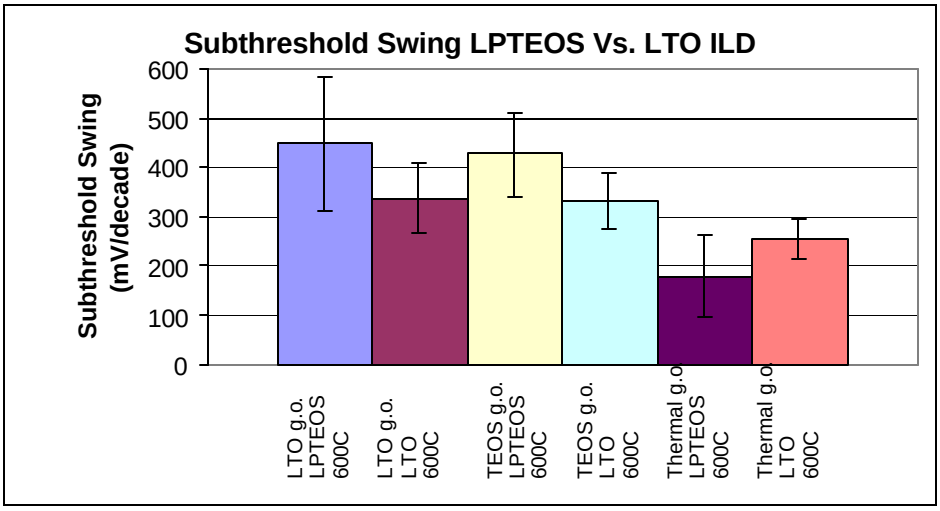

Figure 7.12: Sub-threshold swings for LPTEOS and LTO ILDs with 1s error bars

As shown in Figure 7.12, the low power TEOS ILD results in a higher sub-threshold swing with TEOS and LTO gate oxides. As shown previously with the standard TEOS ILD, the sub-threshold swing was actually smaller for the thermal oxide, reinforcing the hypothesis that available hydrogen was tying up dangling bonds during the deposition.

7.6 Low Power TEOS ILD Annealed at 900°C

A 900°C anneal was given to wafers that received the low power TEOS ILD to determine if the induced damage was reversible. Figures 7.13 and 7.14 show typical I-V curves of wafers that received the low power ILD recipe, followed by a 900°C N_2 anneal.

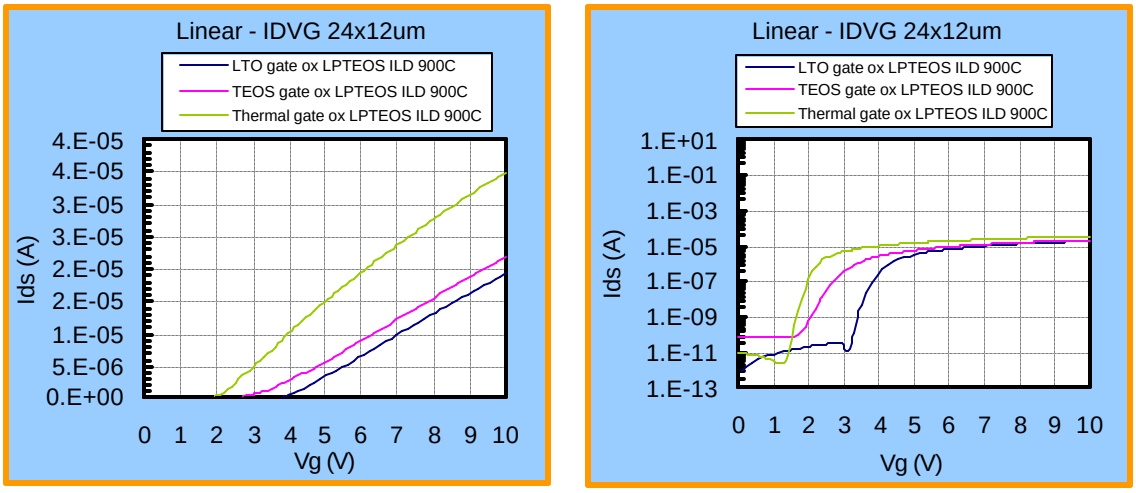

Figure 7.13: Linear I_D-V_G curves for devices with low power TEOS ILD (V_D=0.1V)

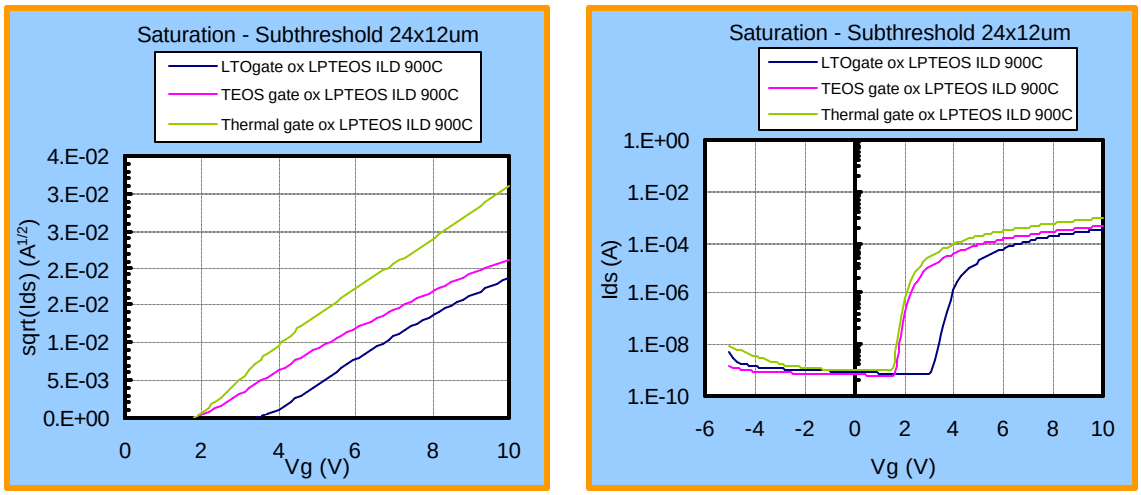

Figure 7.14: Saturation I_D-V_G curves with low power TEOS ILD (V_D=10V)

Although there appears to be a slight threshold voltage shift for the device that has an LTO gate oxide, it cannot be established to be significant, unfortunately, because of the large non-uniformity in the p-well doping (discussed previously). However, the curves in Figures 7.13 and 7.14 do provide valuable insight into the removal of induced damage. In both the linear and saturation mode of operation, I-V curves are smooth with little to no stretching. This shows that the 900°C anneal was adequate in removing the interface states induced by the low power TEOS ILD deposition. Figure 7.15 shows sub-threshold swings for wafers fabricated with the low power TEOS ILD annealed at both 600°C and 900°C.

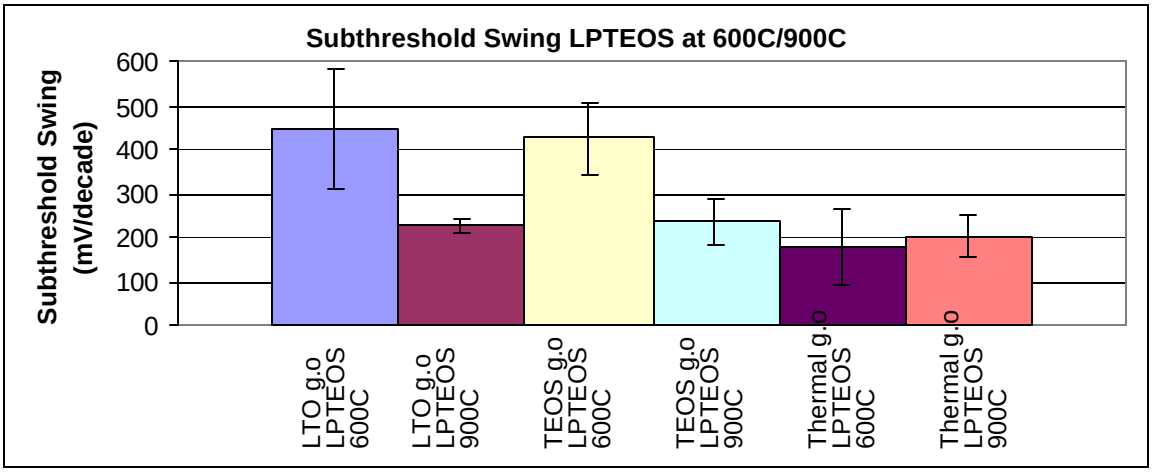

Figure 7.15: Sub-threshold swings for LPTEOS 600°C/900°C with 1s error bars

Sub-threshold swings with LTO ant TEOS gate oxides improved dramatically with the 900°C. Induced interface states from the ILD deposition appear to be adequately removed when the higher temperature anneal is used. For the thermal gate oxide, sub-threshold swing appeared to be slightly higher. This may be from a enhancement in interface states using the 900°C anneal, even though this process was followed by a low-temperature H_2/N_2 sinter.

7.7 Annealing Bulk Charge Damage in LTO Gate Oxides

Devices fabricated with LTO gate oxides with different anneals were used to determine the temperature at which the induced bulk oxide traps are removed. Figures 7.16 and 7.17 show these treatment combinations.

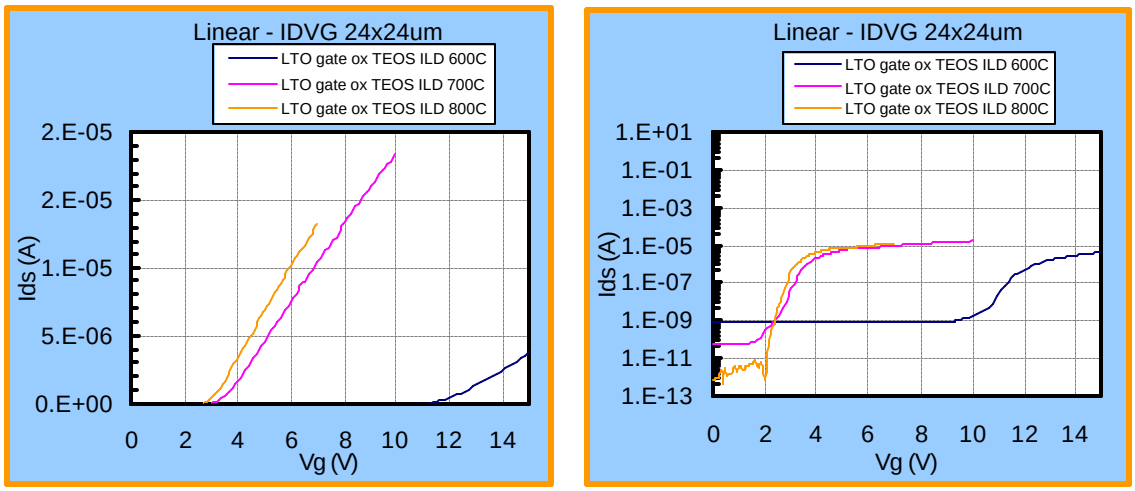

Figure 7.16: Linear I_D-V_G curves for devices with std. TEOS ILD (V_D=0.1V)

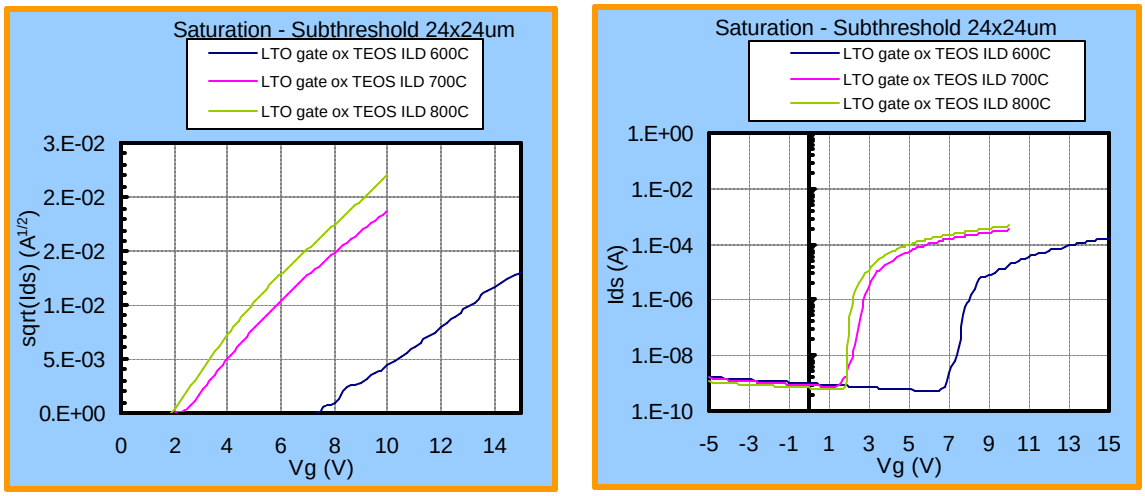

Figure 7.17: Saturation I_D-V_G curves with std. TEOS ILD (V_D=10V)

Figures 7.16 and 7.17 show that a 700°C anneal is adequate in removing the majority of the bulk oxide charge induced in the LTO gate oxide. The wafer annealed at 900°C showed a further decrease in threshold voltage as well as minor improvement in sub-threshold slope. Also, the data taken in the linear regime and plotted on a log scale showed improvements in off-state leakage currents for devices annealed at the higher temperatures.

CHAPTER 8
CONCLUSION

MOS capacitors and NMOS transistors were successfully fabricated with different gate oxides, different ILDs and different annealing temperatures in order to show specific susceptibilities to plasma induced charge damage. Despite the oxidized molybdenum with wafers containing the TEOS ILD annealed at 900°C, valuable insight was obtained from the remaining treatment combinations. It was shown that when an oxide undergoes field-induced stress, such as in a plasma, an increase and slight redistribution of interface states results. Such effects result in different types of stretching in C-V and I-V characteristics. In addition to demonstrating interfacial damage, bulk oxide charge trapping was also observed with the LTO gate oxide.

8.1 Properties of the TEOS Gate Oxide

It was found that the PECVD gate oxide is the most vulnerable to interface degradation when exposed to a plasma process or applied field. When annealed at 600°C and exposed to stress, the TEOS gate oxide showed a drastic increase in interface states when measured by C-V. After exposure to the stress, the TEOS gate oxide showed a much larger increase trap states near mid-gap compared to the thermal and LTO gate oxides (Figure 35a). In agreement with the demonstration of a comparably weak interface for the TEOS gate oxide, both C-V and I-V curves showed a drastic degree of stretching on wafers exposed to plasma in the ILD deposition. When the standard TEOS ILD recipe was used, the stretching of the I-V curve was different than those of transistors fabricated with LTO and thermal gate oxides. This has been attributed to an elevated number of mid-gap interface states as a result of process induced stress.

Mobile ionic species measured in the TEOS oxide showed that without an anneal, it contained nearly an order of magnitude more charge than the thermal and LPCVD-oxide. It was also shown that there was more than one species of mobile charge present, as TVS data exhibited multiple capacitance peaks with the TEOS-oxide. One of these mobile ions appeared become trapped or gettered by a high temperature furnace anneal.

When the TEOS gate oxide is annealed at 900°C, a higher quality interface is achieved resulting in a decreased vulnerability to process-induced damage. This was first observed in capacitors given interface trap density distribution measurements before and after exposure to a stress. Interface trap distributions of TEOS gate oxides annealed at 900°C were similar to those of LTO when a stress was applied. It was also found that the high temperature anneal restored sub-threshold slopes in the I-V curves of transistors containing TEOS gate oxides annealed at 900°C. The results summarizing observed damages to the TEOS gate oxide are shown below in Figure 8.1. These effects were best shown in saturation on a log scale.

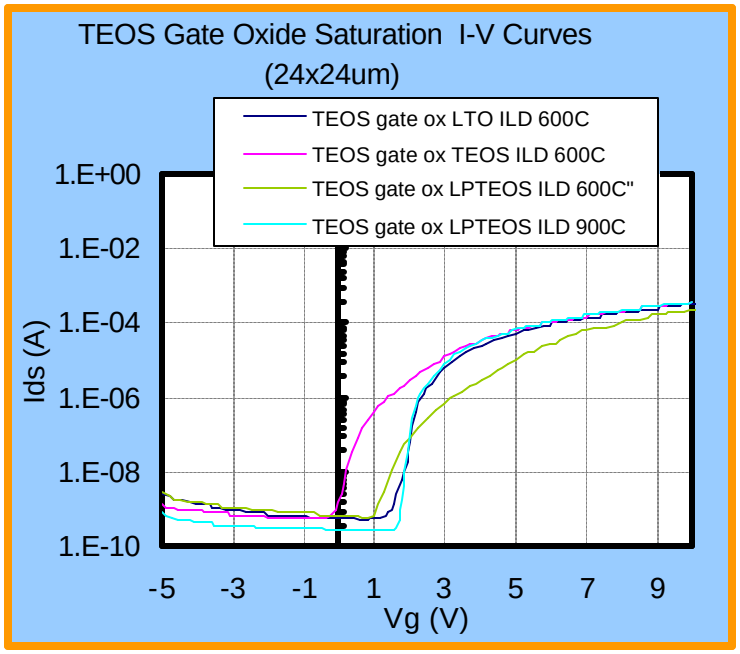

Figure 8.1: I-V data summarized for the TEOS gate oxide

8.2 Properties of the LTO Gate Oxide

LTO gate oxides suffered from bulk oxide charging when exposed to plasma during the ILD deposition process. When annealed at 600°C, charge remained in the bulk of the gate oxide causing a large threshold voltage shift. This was expected after comparatively high leakage currents were demonstrated with MOS capacitors. A noticeable amount of interfacial damage was also observed at the low process temperature. Both C-V and I-V curves showed stretching and distinct kinks resulting from induced trap states.

The 900°C anneal proved to be adequate in removing the interfacial damage that was induced in the TEOS ILD deposition. This was best demonstrated with devices that received the low power TEOS ILD deposition. Damage observed as a result of bulk oxide trapping was removed with the 700°C and 800°C anneals. Data showed clear restoration of the expected threshold voltage with wafers receiving the higher temperature anneals. Figure 8.2 below shows a summary of the observed damage observed with LTO gate oxides.

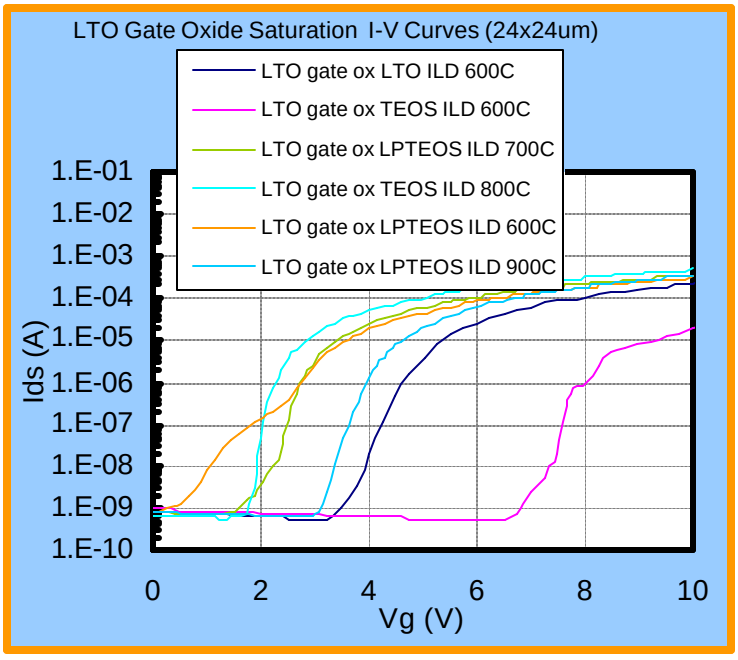

Figure 8.2: I-V data summarized for LTO gate oxides

8.3 Properties of the Thermal Gate Oxide

The thermal gate oxide showed an increase in interface trap density distributions after exposure to stress subsequent to fabrication. However, electrical data showed compression in both C-V and I-V data when exposed to plasma during processing. This would normally be characteristic of reduced or low levels of interface states. The ILD deposition may have acted like a sinter for the thermal oxide. Remaining hydrogen atoms combined with an elevated temperature of 390C could make such behavior possible. A sintering effect is consistent with the observation that the low power TEOS ILD treatment combinations demonstrate the best sub-threshold performance; there was a decreased field dropped across the interface and it was exposed to the elevated temperature and hydrogen ions for a longer (relative) period of time with the low power ILD recipe. This is demonstrated in the summary of I-V curves in Figure 8.3. As described, the curve from the wafer exposed to the low power TEOS ILD had the best sub-threshold swing and interfacial integrity.

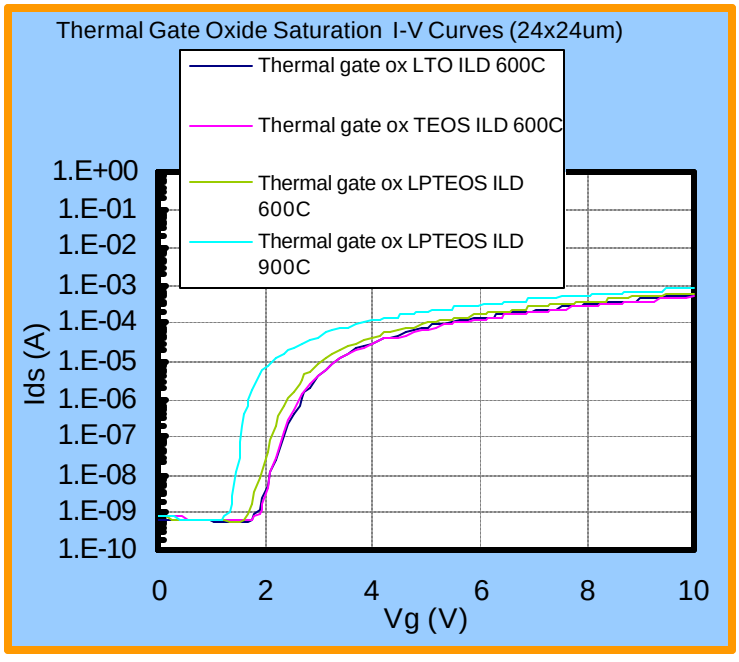

Figure 8.3: I-V data summarized for thermal gate oxides

8.4 Low Power vs. High Power TEOS ILD

Decreasing the power in the ILD deposition was successful in eliminating bulk charging in the LTO gate oxide. The lower power resulted in a decreased field across the gate oxide during deposition, minimizing the amount electrons that could become trapped. However, because the power was lower, the deposition rate was significantly decreased. As a result of this, the gate oxide was exposed to the plasma for a much longer period of time and more interfacial damage resulted for the PECVD and LPCVD oxides. On the contrary, thermal oxides appeared to prefer the lower deposition power, as decreased sub-threshold swings were observed.

8.5 Closing Remarks

As far as gate dielectrics, the LTO oxide is still considered to be the low temperature oxide of choice at RIT. It exhibits less total charge and interface states than the TEOS-oxide. Although it does leak more current making it more susceptible to bulk trapping, it is not a major concern as LTO oxide can be effectively used as the ILD in the fabrication process.

If a PECVD ILD must be used in the low temperature process, a pre-plasma anneal would most likely be effective in decreasing the degree of interfacial damage to a TEOS-oxide. If a PECVD ILD must be used with an LTO oxide at low process temperatures, an optimal deposition power should be determined in order to balance the trade-off between the induced interface states and bulk trapping observed in the experiment. A furnace clean may also be adequate in removing the contamination that induces high leakage currents and susceptibility to bulk oxide charging.

For high temperature processes, the ILD deposition does not appear to induce lasting levels of bulk charge or interface damage. It does however appear that a low power deposition can result in a sintering effect. For this reason, the low power ILD deposition is preferred when a thermal gate oxide is used.

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